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FIG. 1 (a)

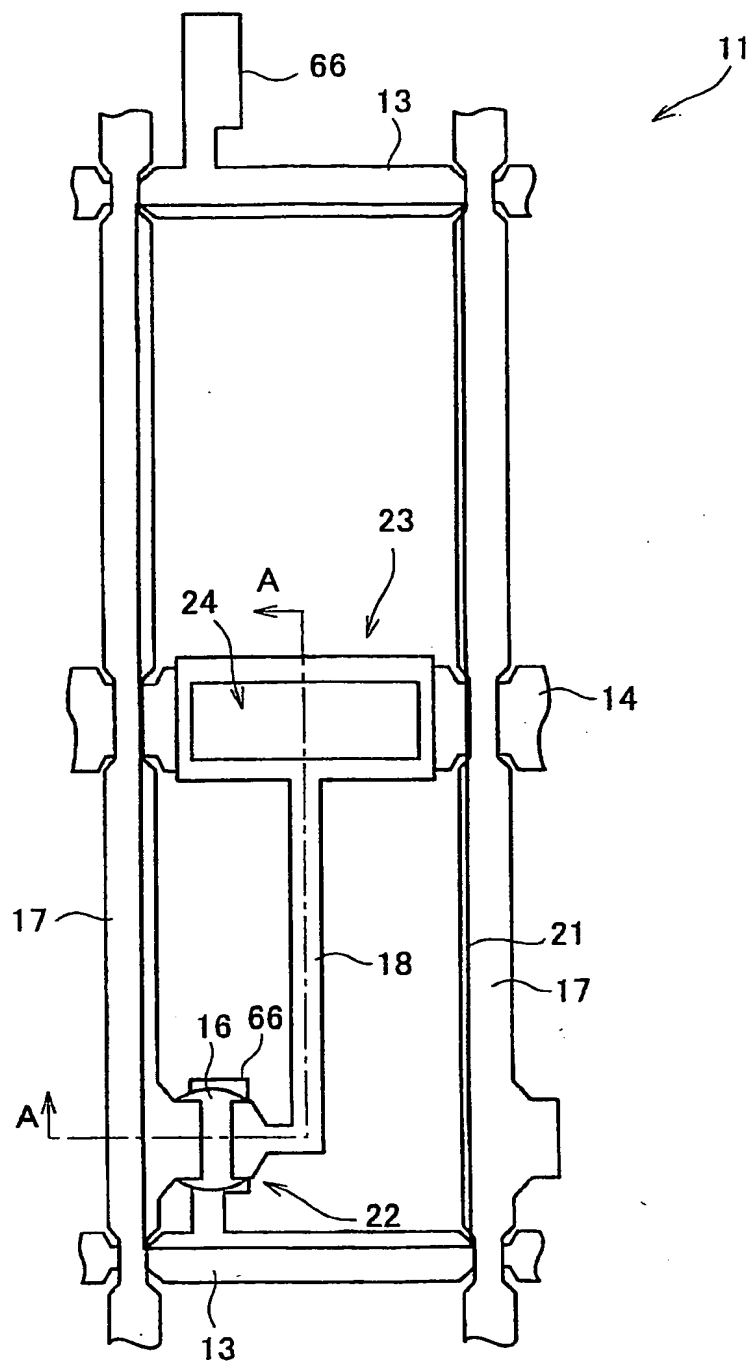


FIG. 1 (b)

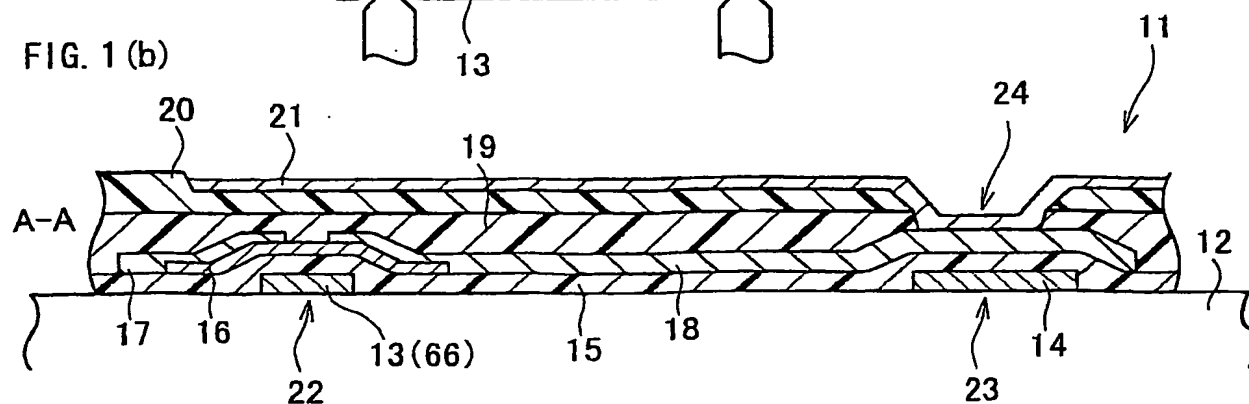


FIG. 2

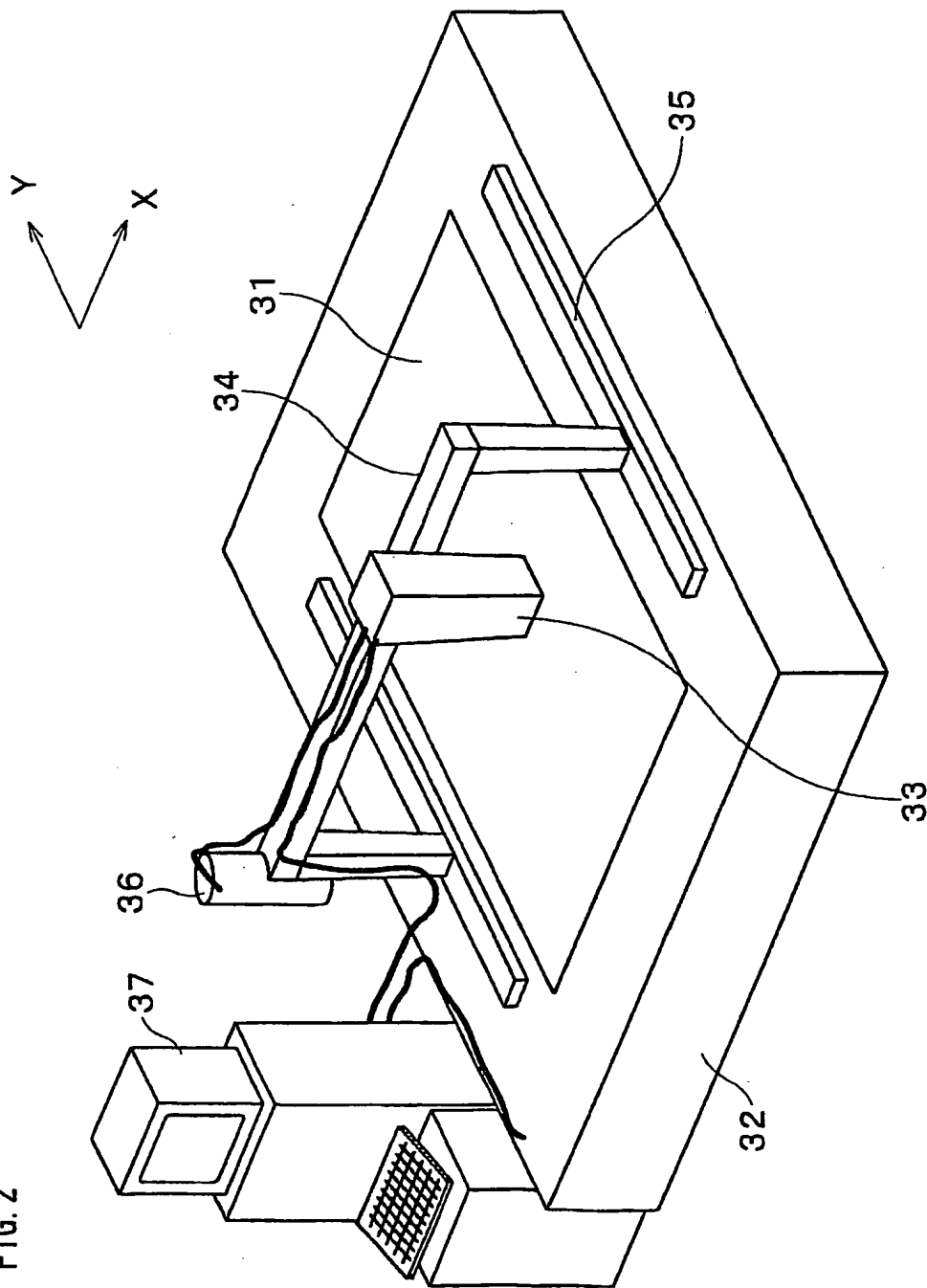


FIG. 3

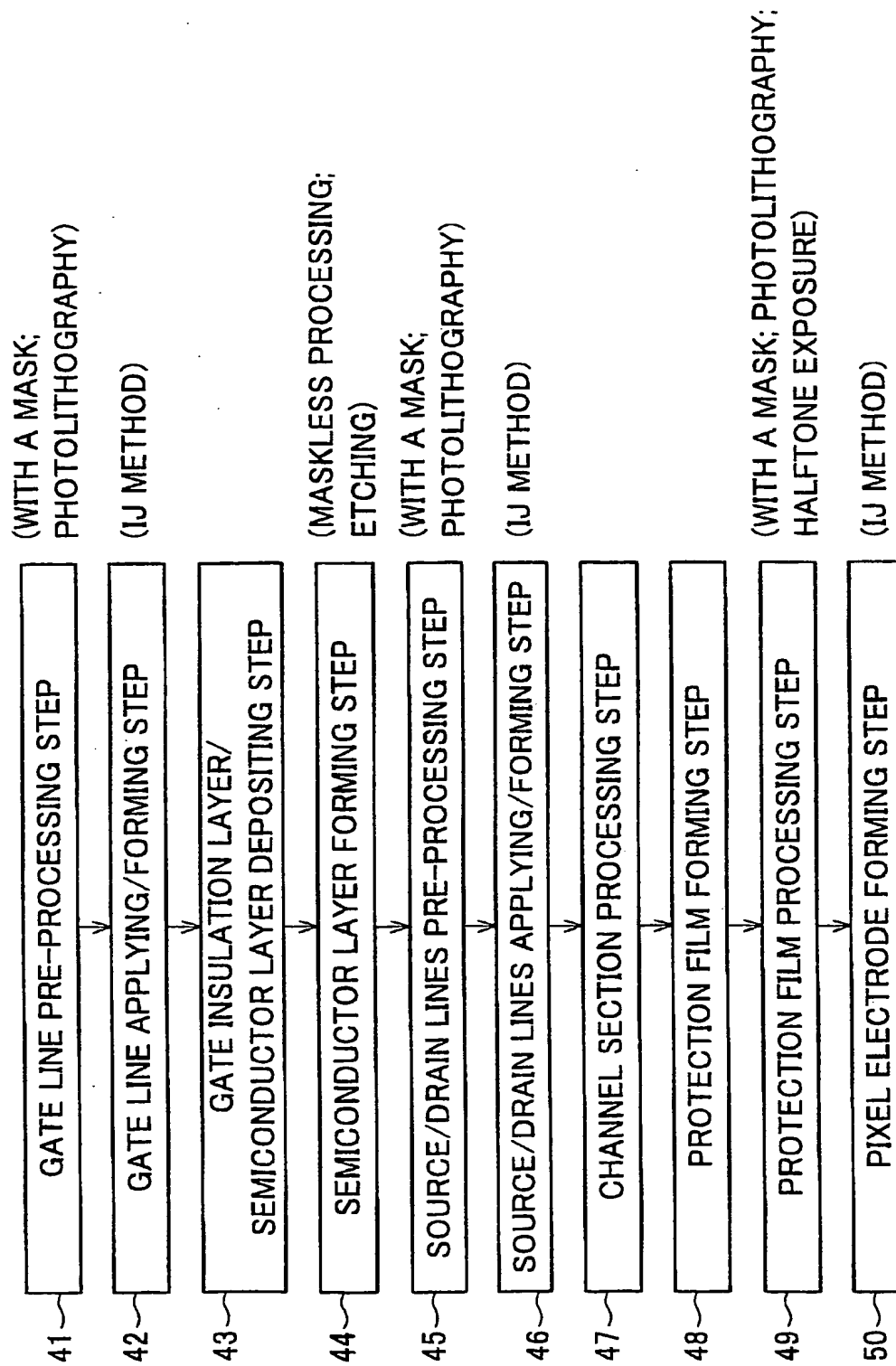


FIG. 4(a) (GATE LINE PRE-PROCESSING STEP)

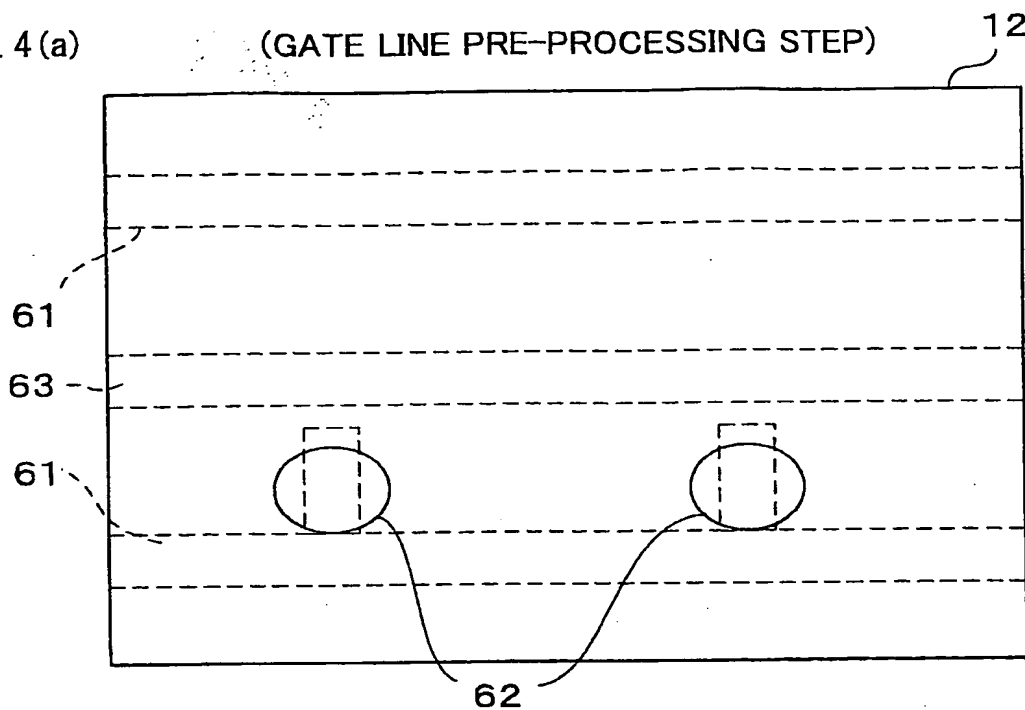


FIG. 4(b) (GATE LINE APPLYING/FORMING STEP)

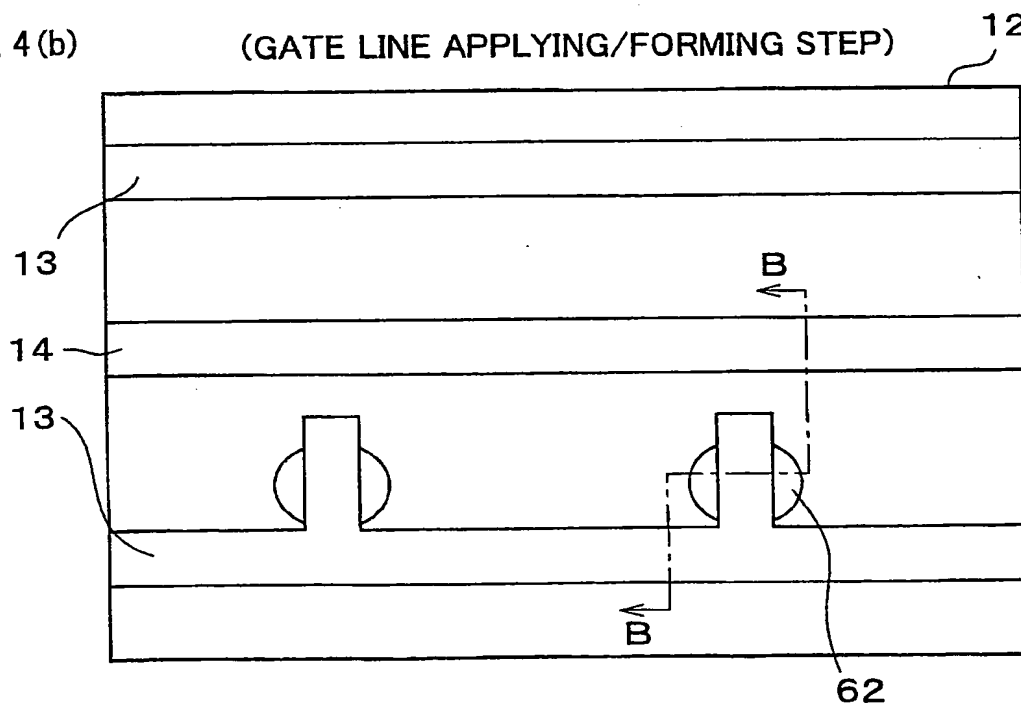
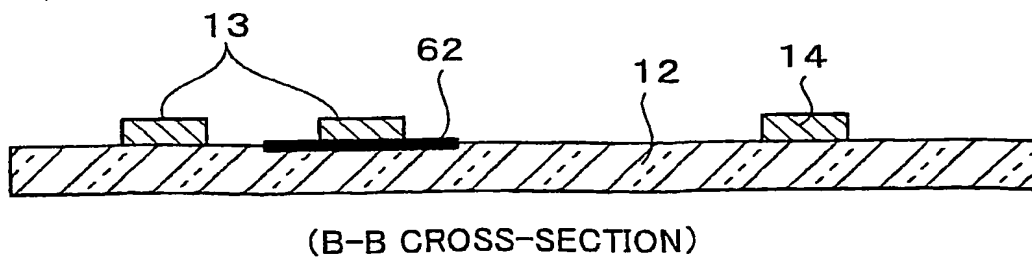


FIG. 4(c)



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FIG. 5(a) (SEMICONDUCTOR FORMING STEP)

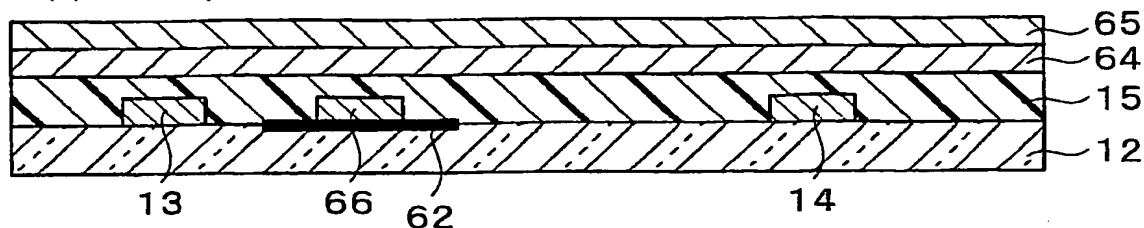


FIG. 5(b)

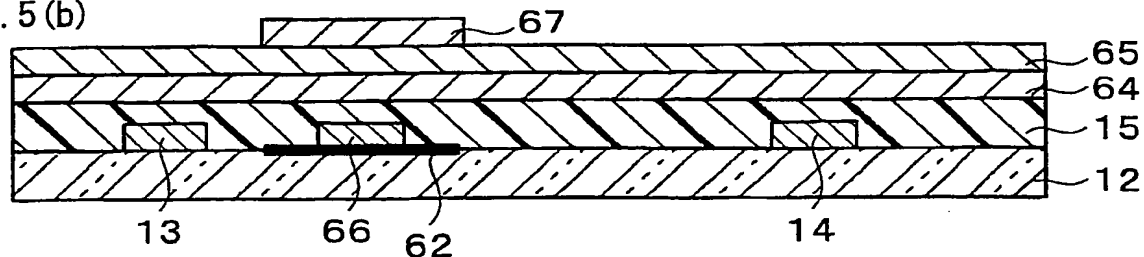


FIG. 5(c)

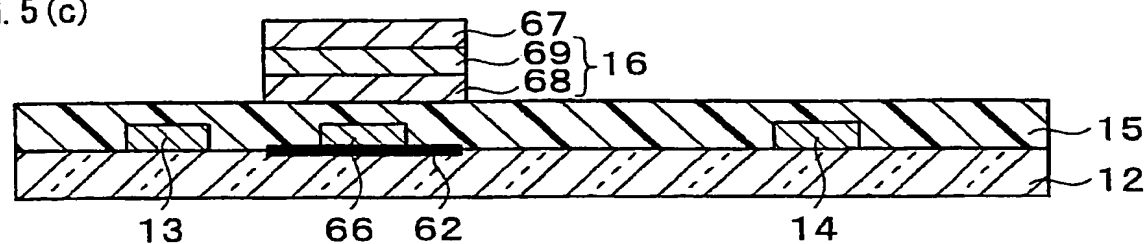
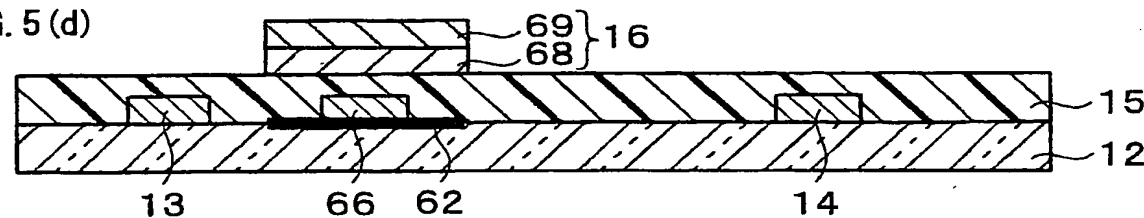


FIG. 5(d)



(C-C CROSS-SECTION)

FIG. 5(e)

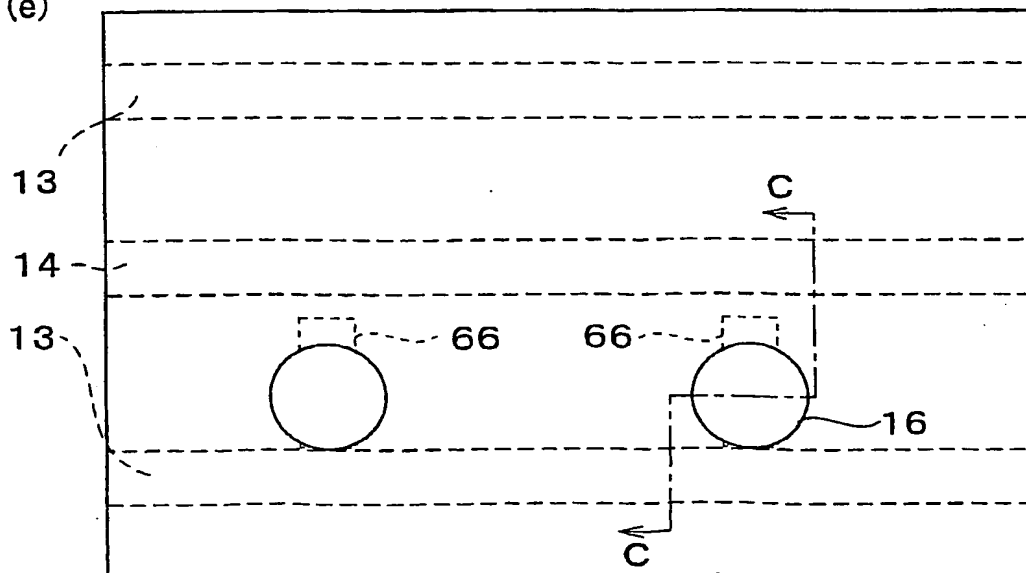


FIG. 6(a) (SOURCE/DRAIN LINES PRE-PROCESSING STEP)

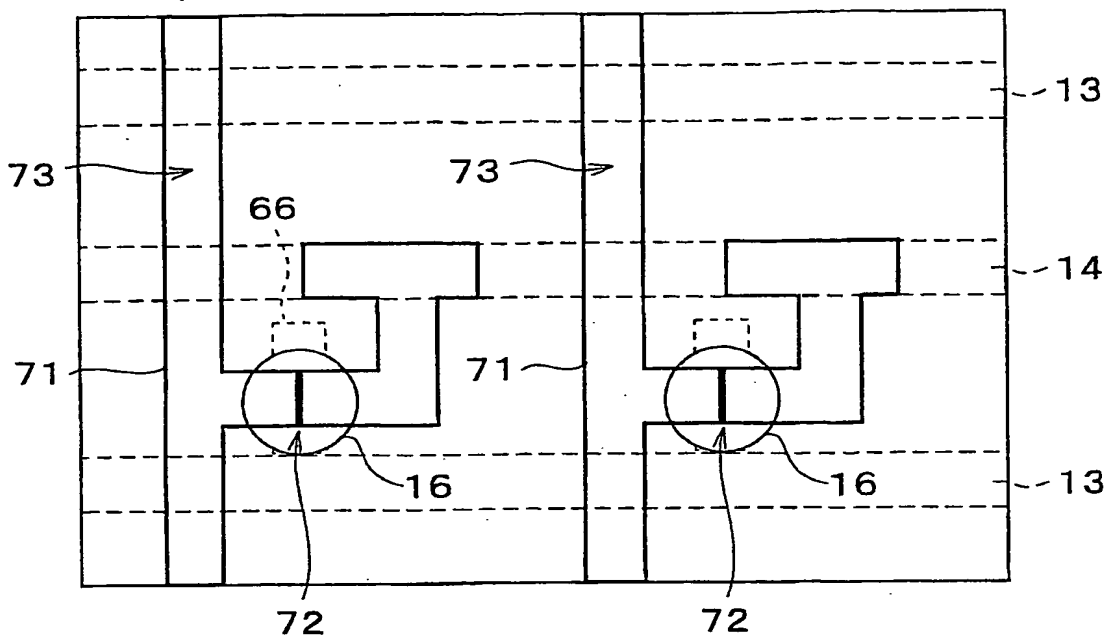


FIG. 6(b) (SOURCE/DRAIN LINES APPLYING/FORMING STEP)

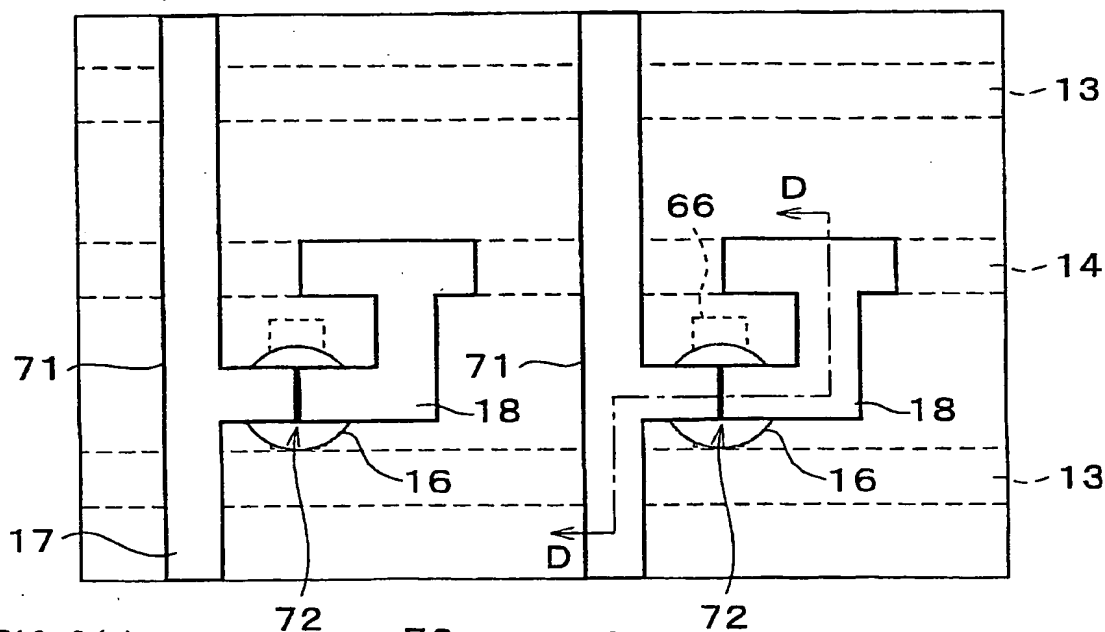
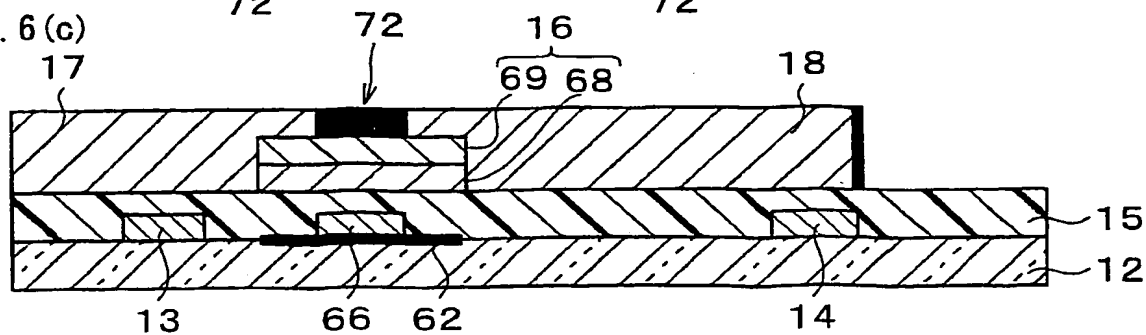


FIG. 6(c)



(D-D CROSS-SECTION)

FIG. 7

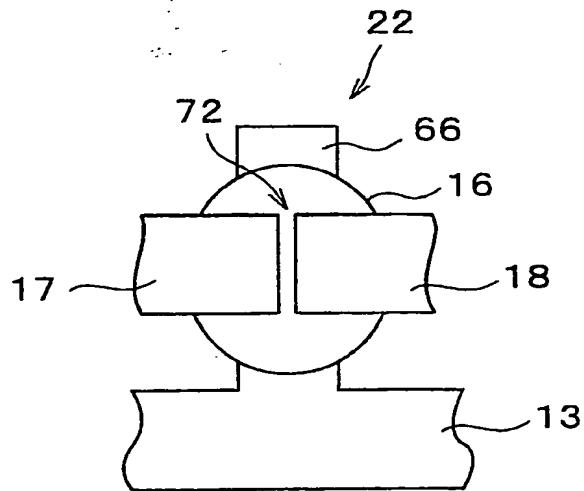


FIG. 8(a)

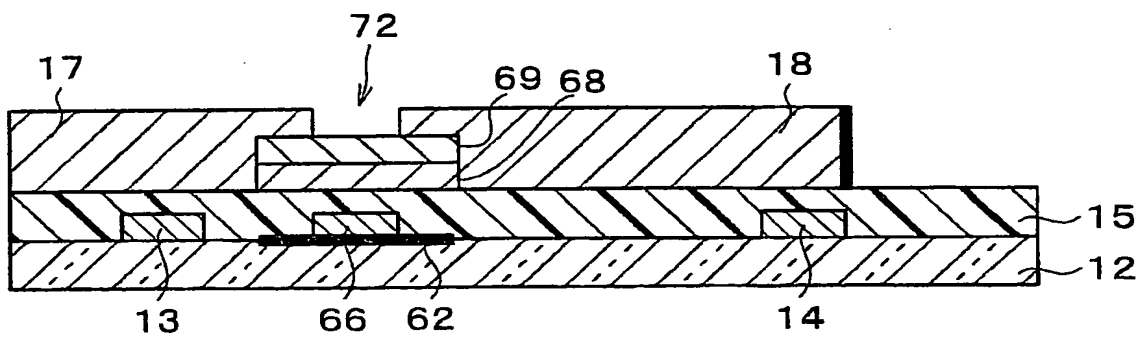


FIG. 8(b)

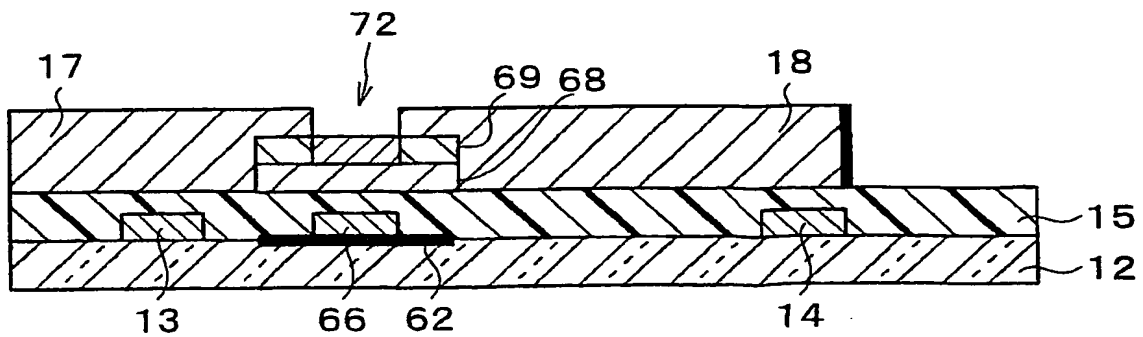


FIG. 9(a)

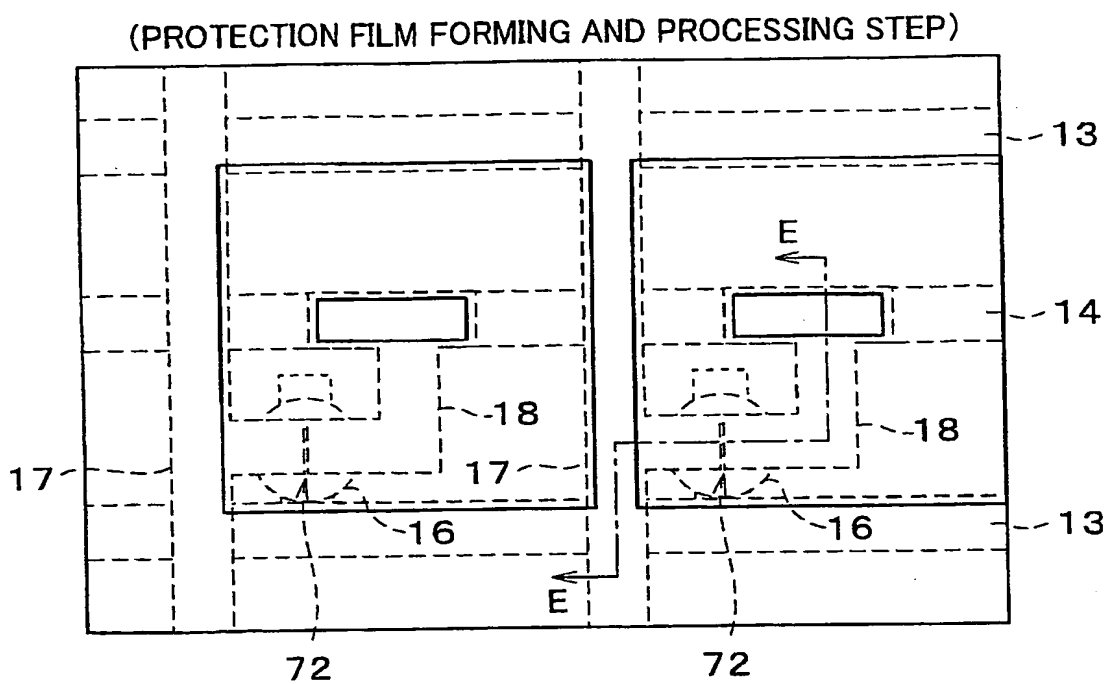
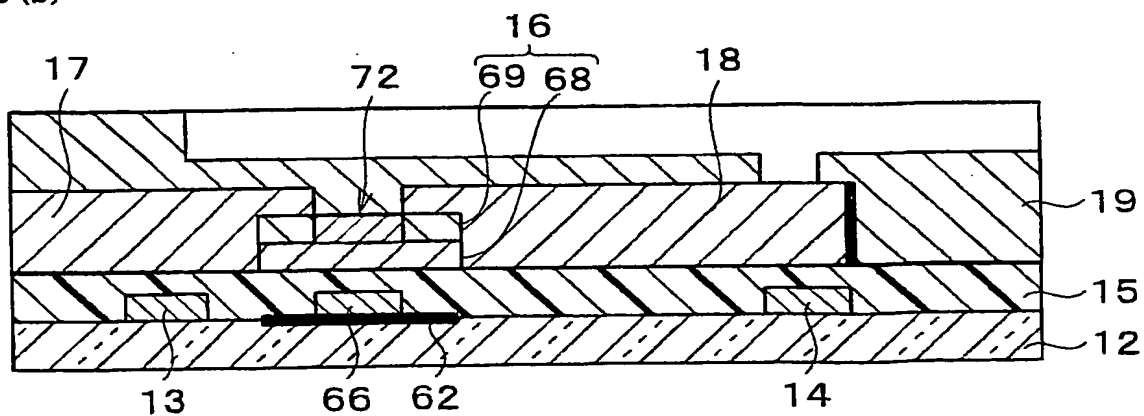


FIG. 9(b)



(E-E CROSS-SECTION)

FIG. 10(a)

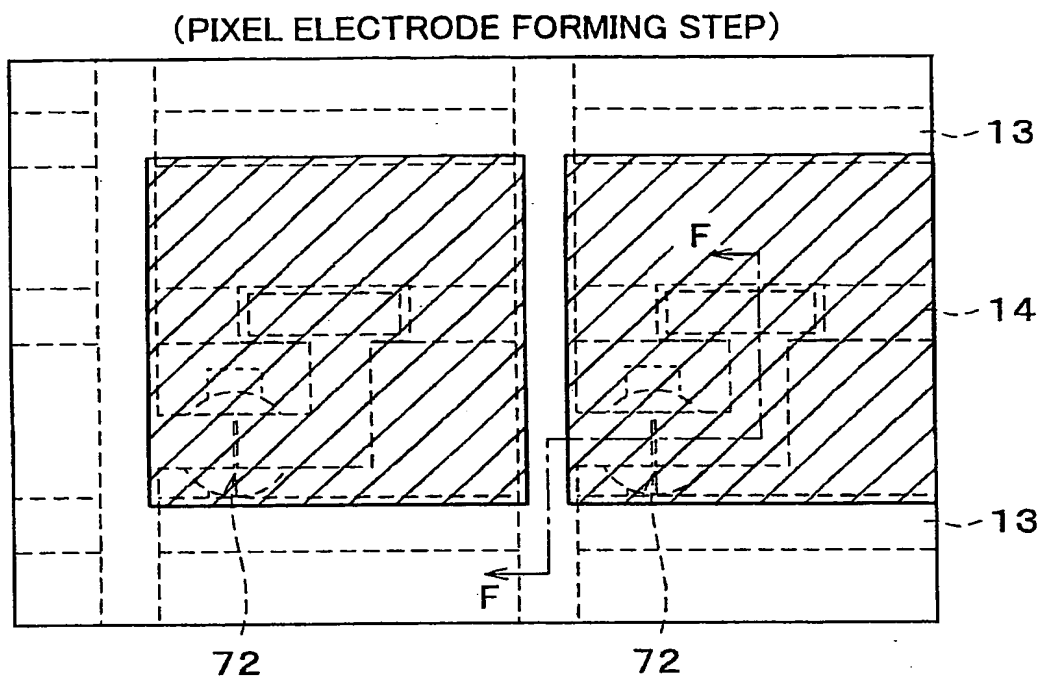
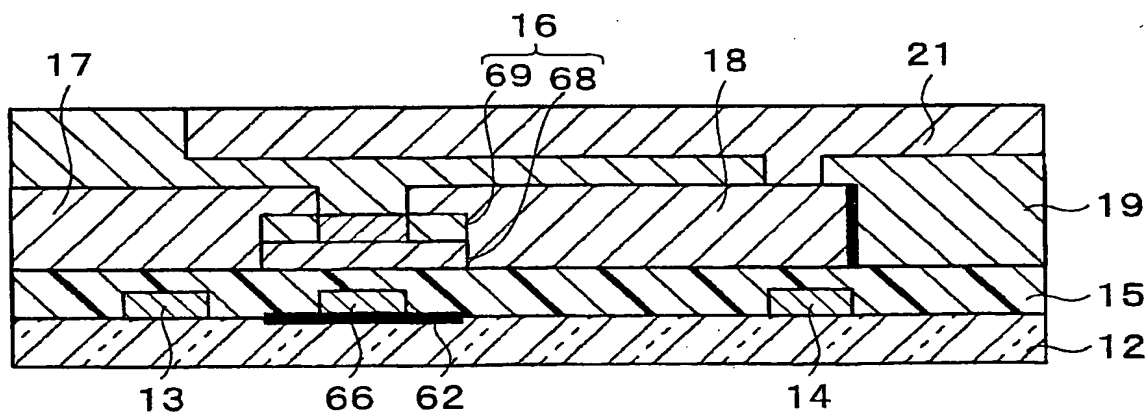


FIG. 10(b)



(F-F CROSS-SECTION)

FIG. 11(a)

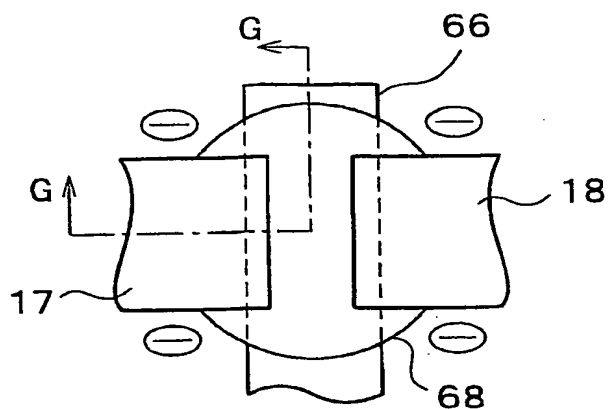
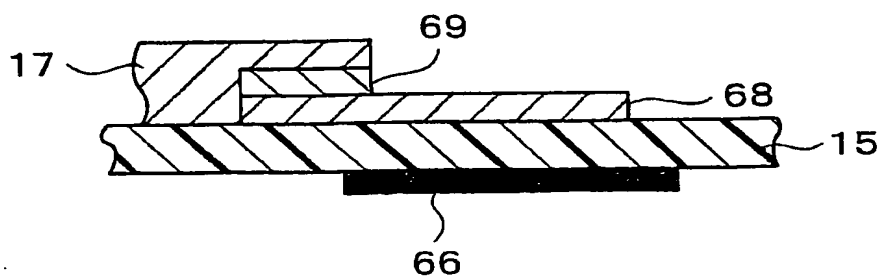


FIG. 11(b)



(G-G CROSS-SECTION)

FIG. 12(a)

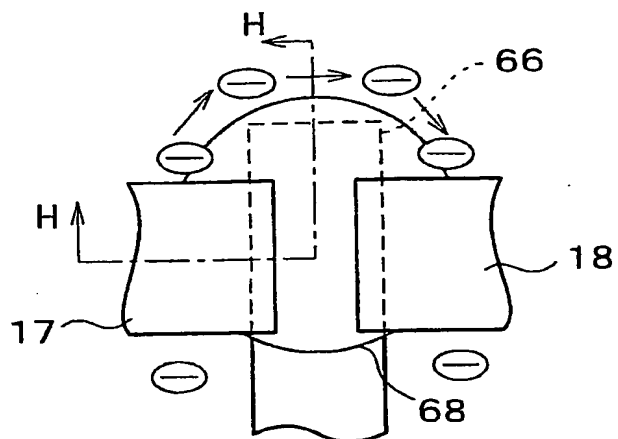
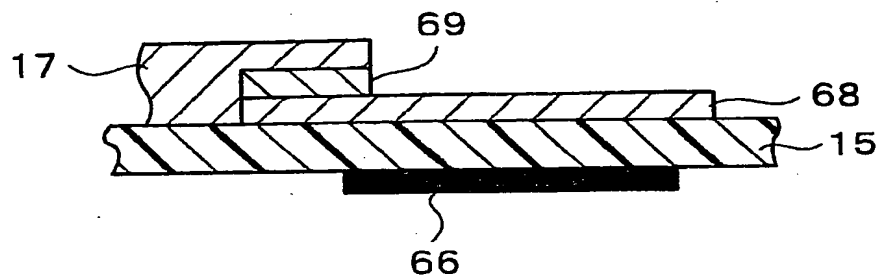
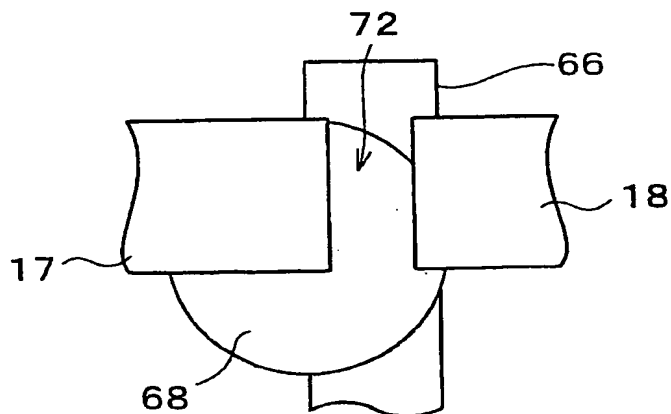


FIG. 12(b)



(H-H CROSS-SECTION)

FIG. 13



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FIG. 14(a)

(CHANNEL SECTION PROCESSING IS COMPLETED)

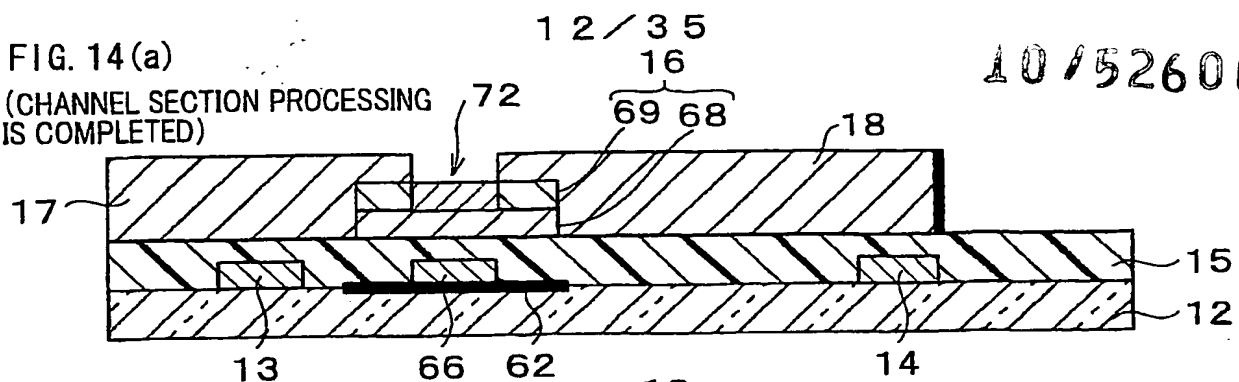


FIG. 14(b)

(LIGHT BLOCKING FILM IS APPLIED)

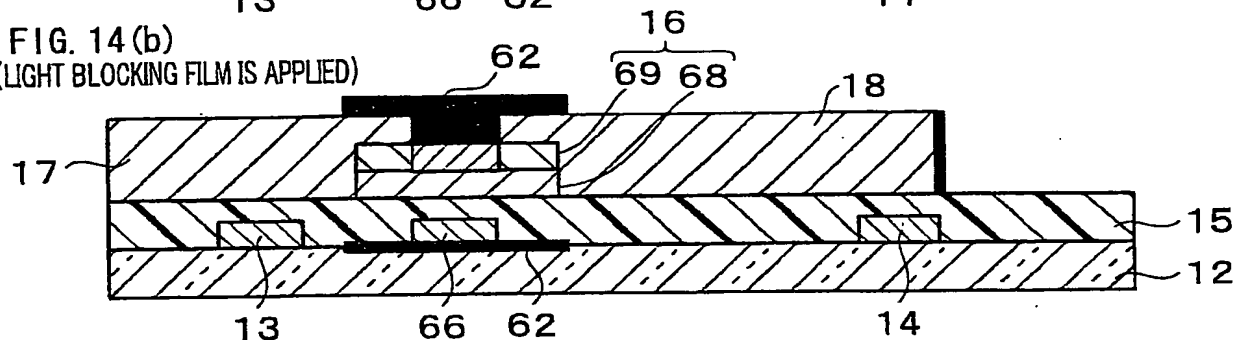
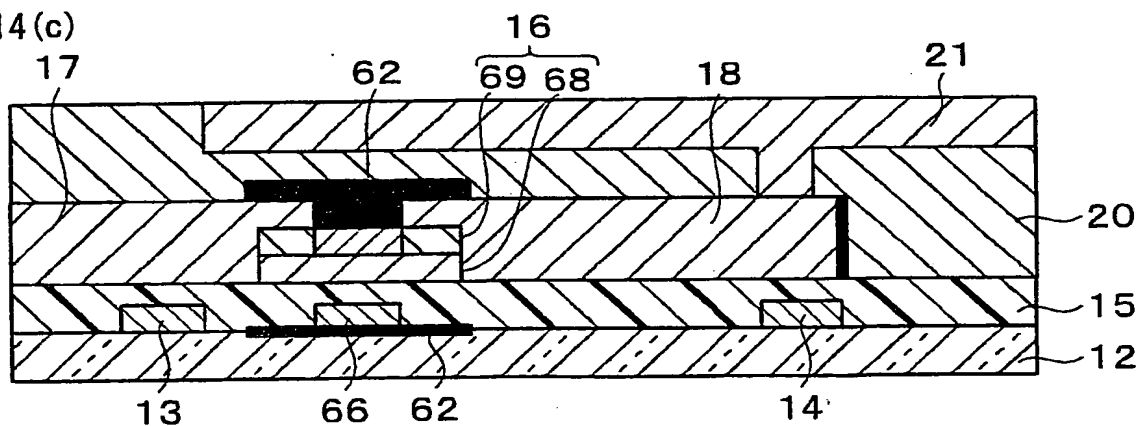


FIG. 14(c)



(M-M CROSS-SECTION)

FIG. 14(d)

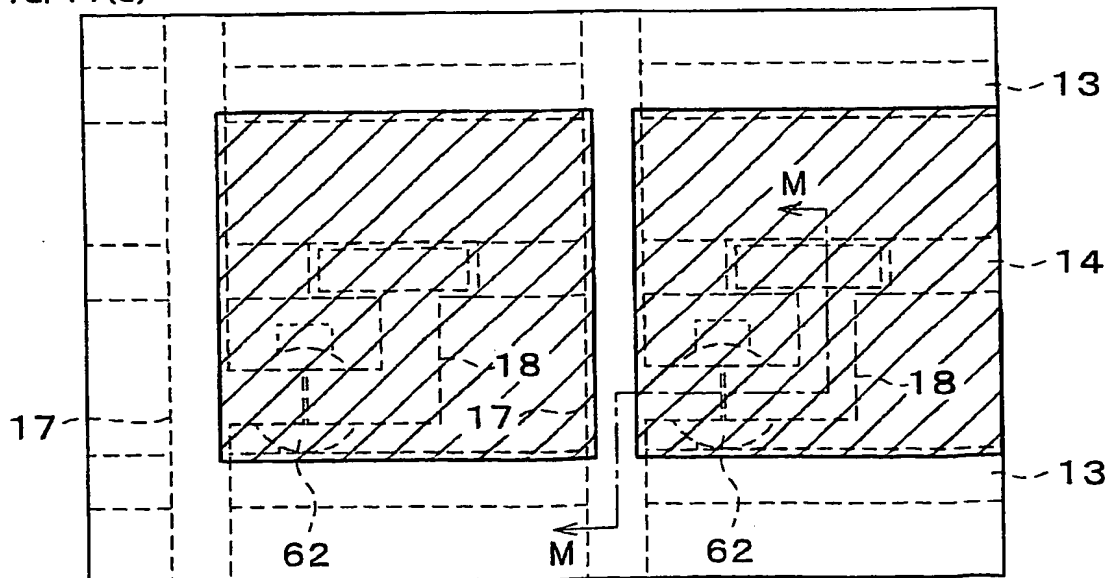


FIG. 15(a)

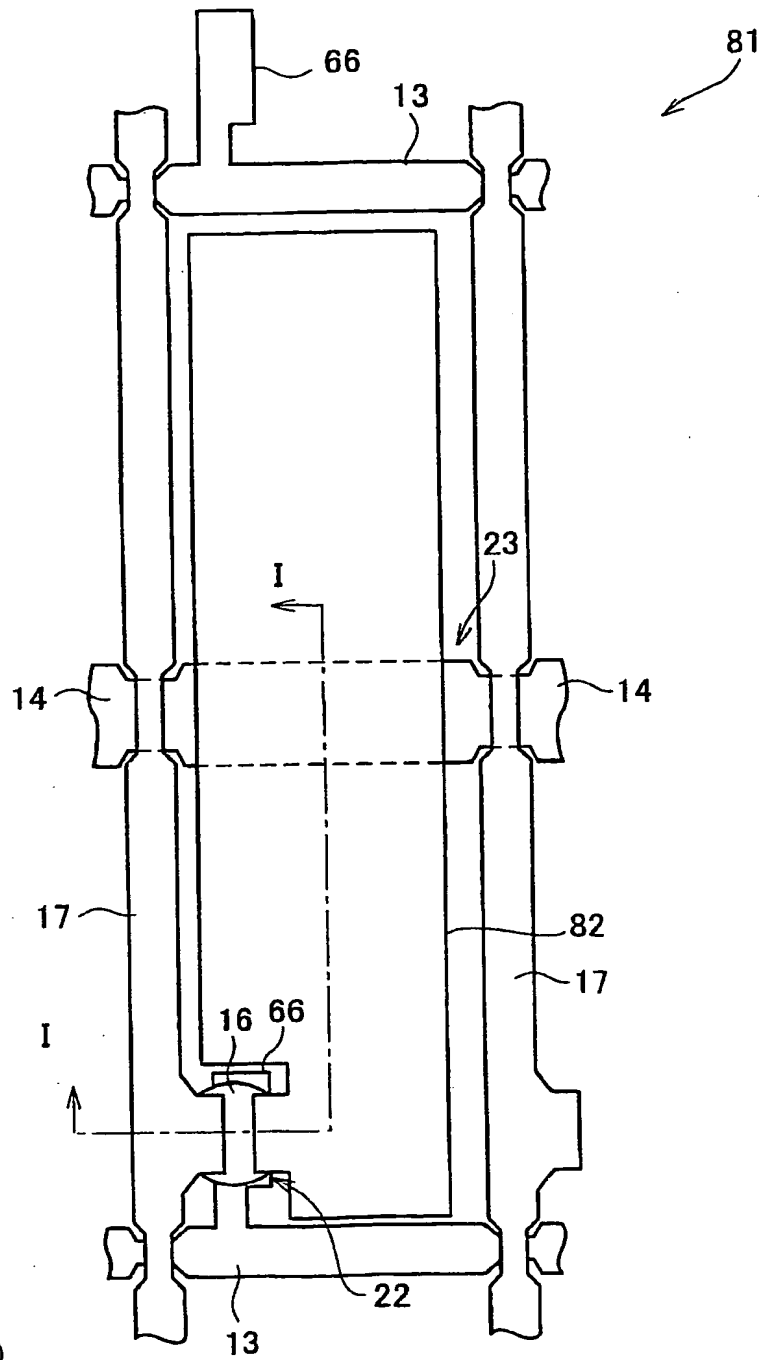


FIG. 15(b)

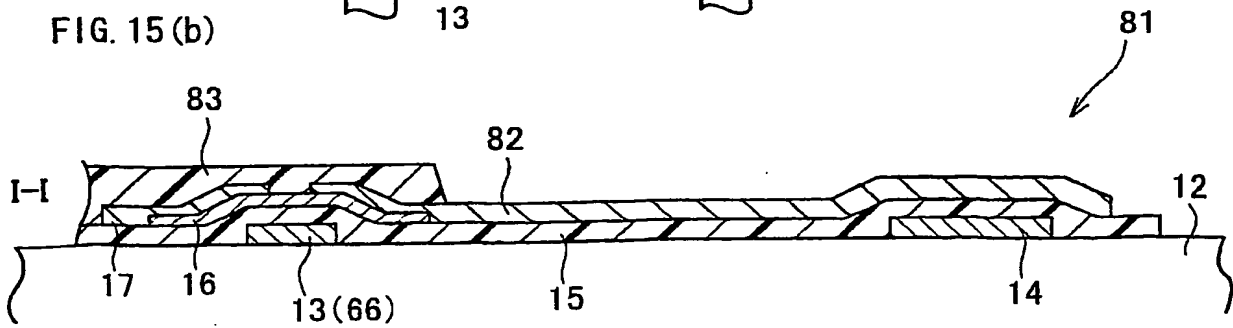


FIG. 16

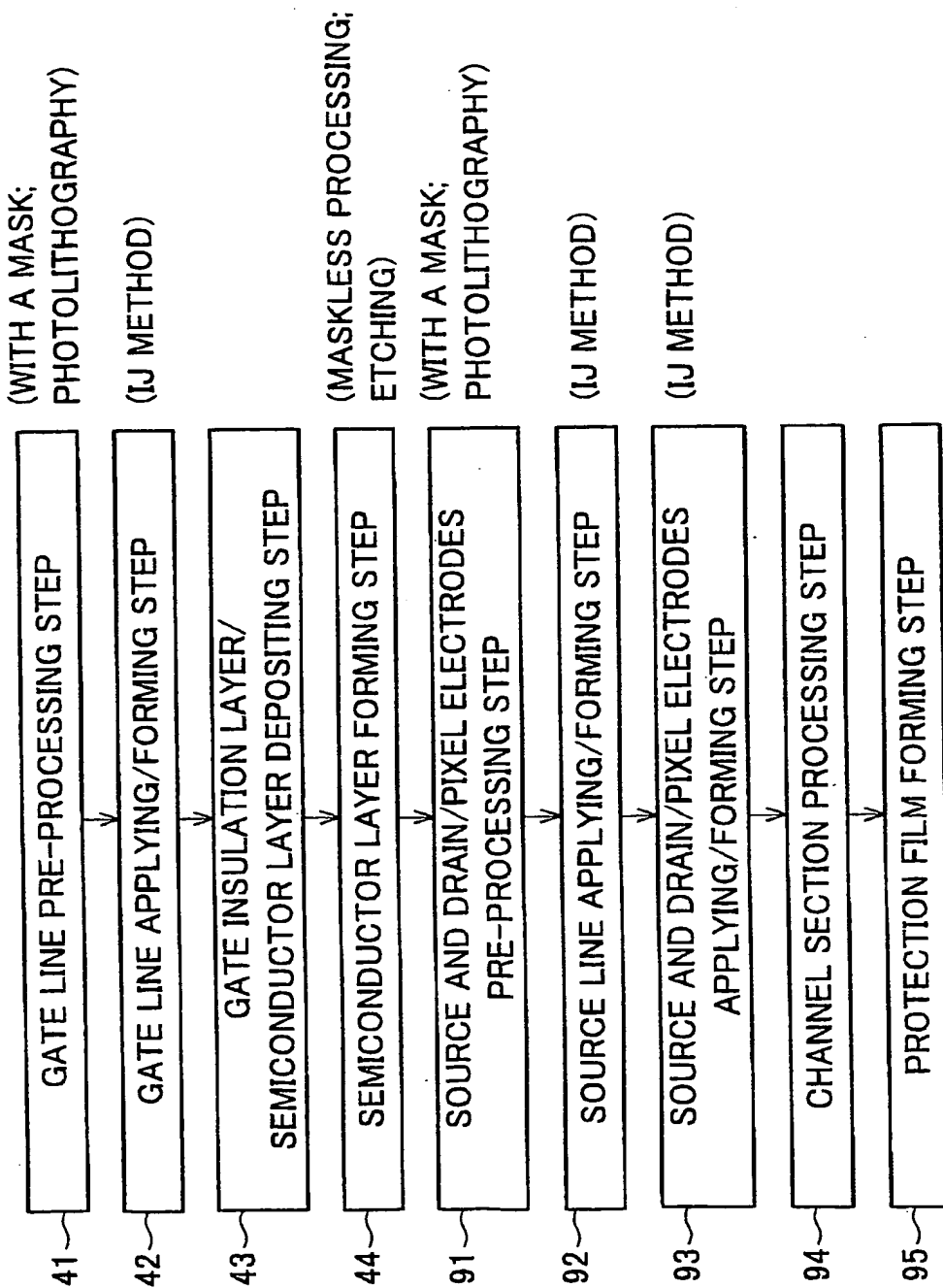


FIG. 17

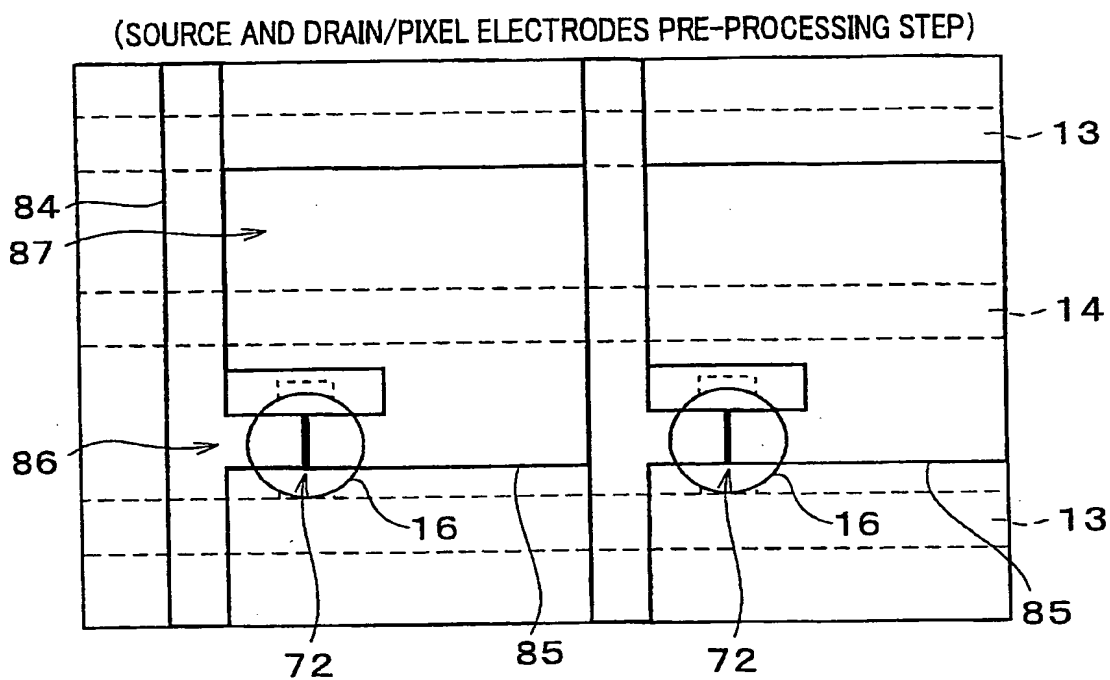


FIG. 18(a)

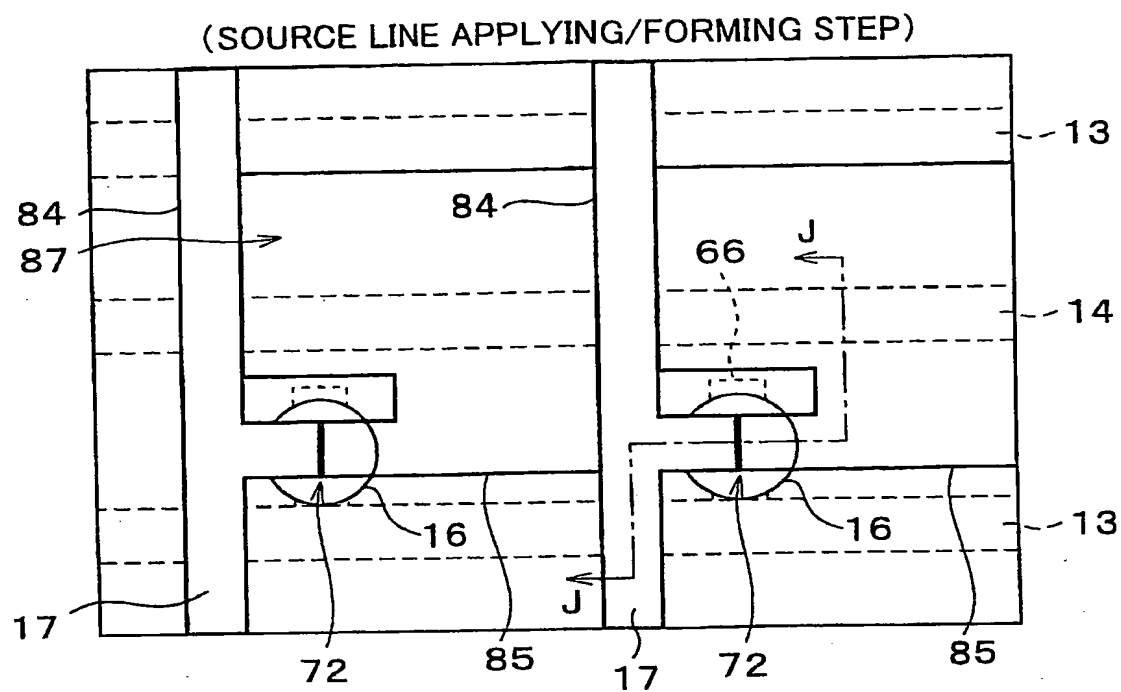


FIG. 18(b)

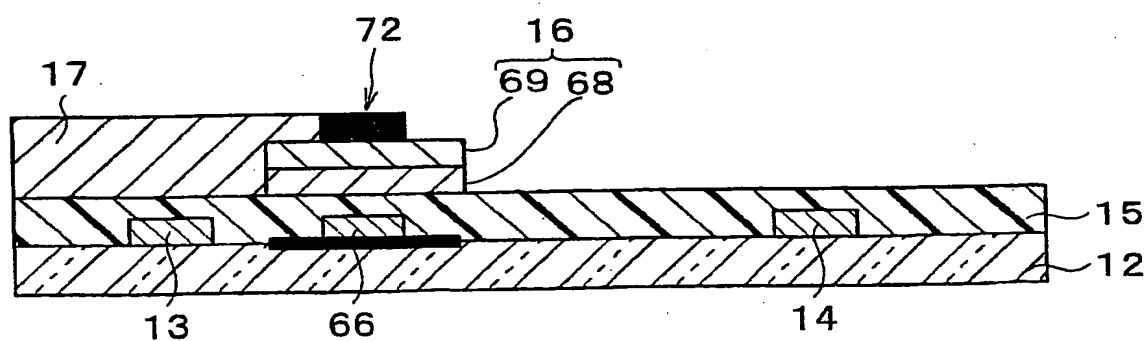


FIG. 19(a)

FIG. 20(a) (CHANNEL SECTION PROCESSING STEP)

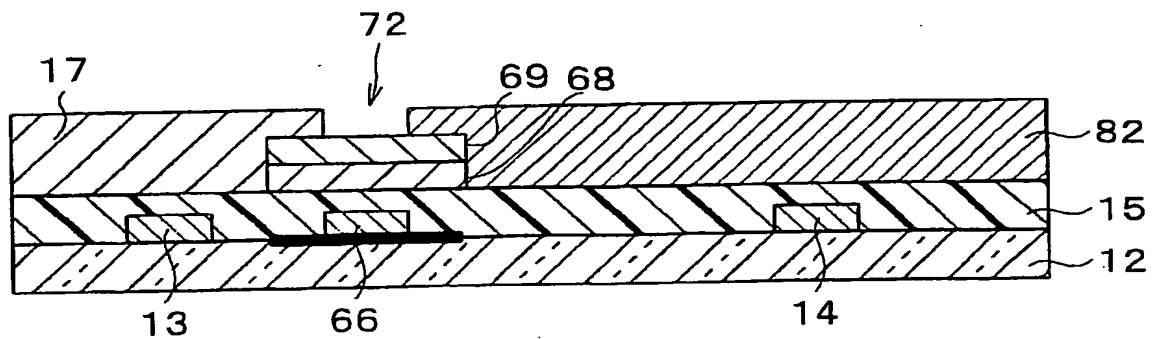


FIG. 20(b)

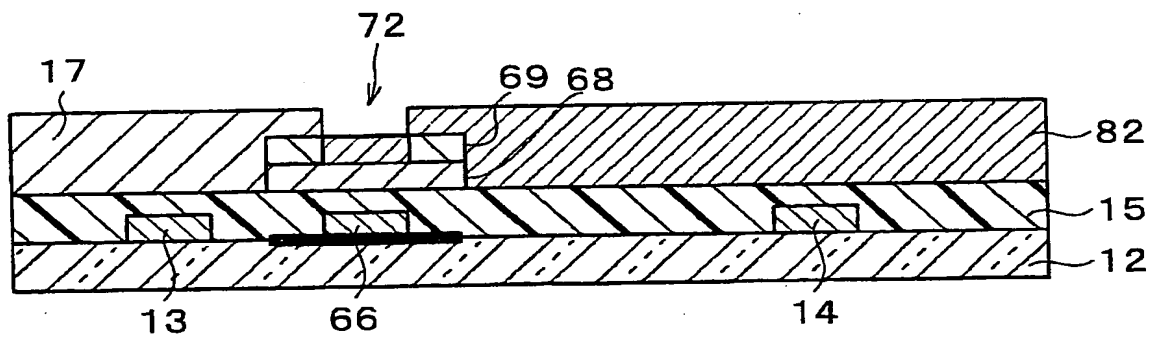


FIG. 21

(PROTECTION FILM FORMING STEP)

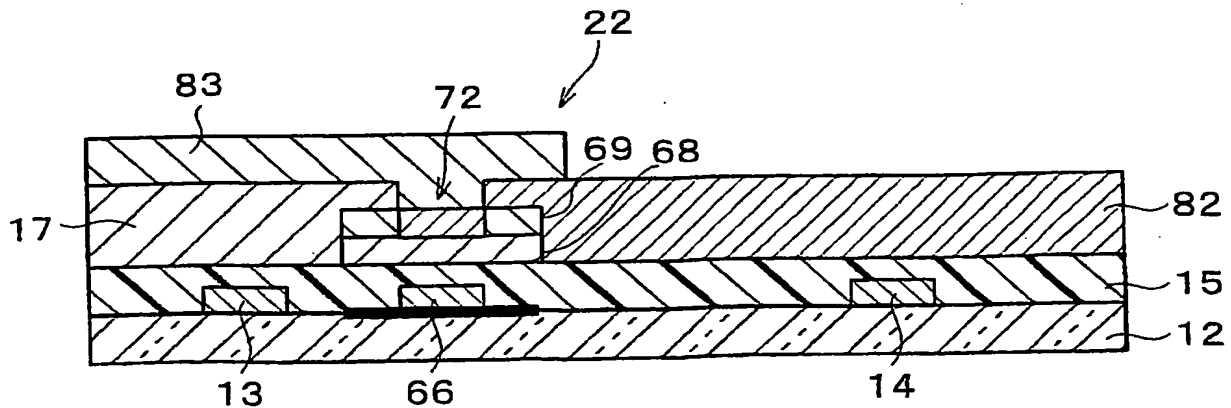


FIG. 22(a)

(SEMICONDUCTOR LAYER FORMING STEP (DIRECT FORMING))

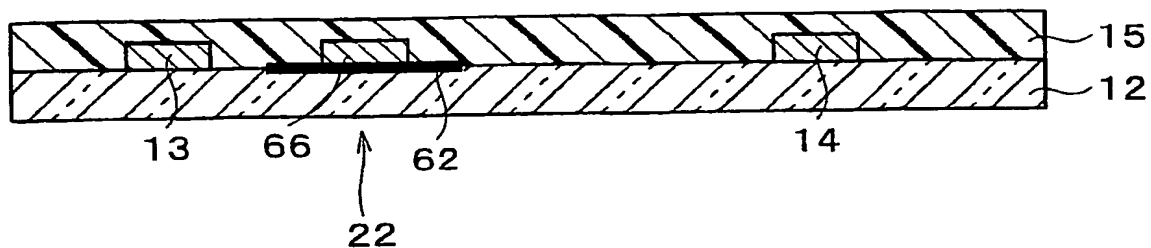


FIG. 22(b)

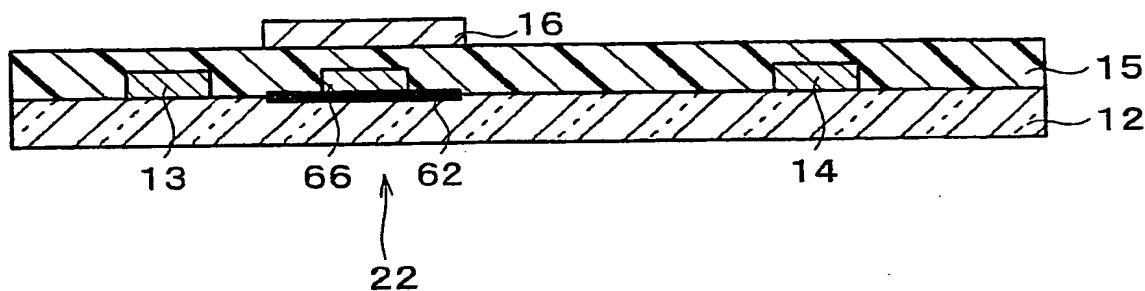


FIG. 22(c)

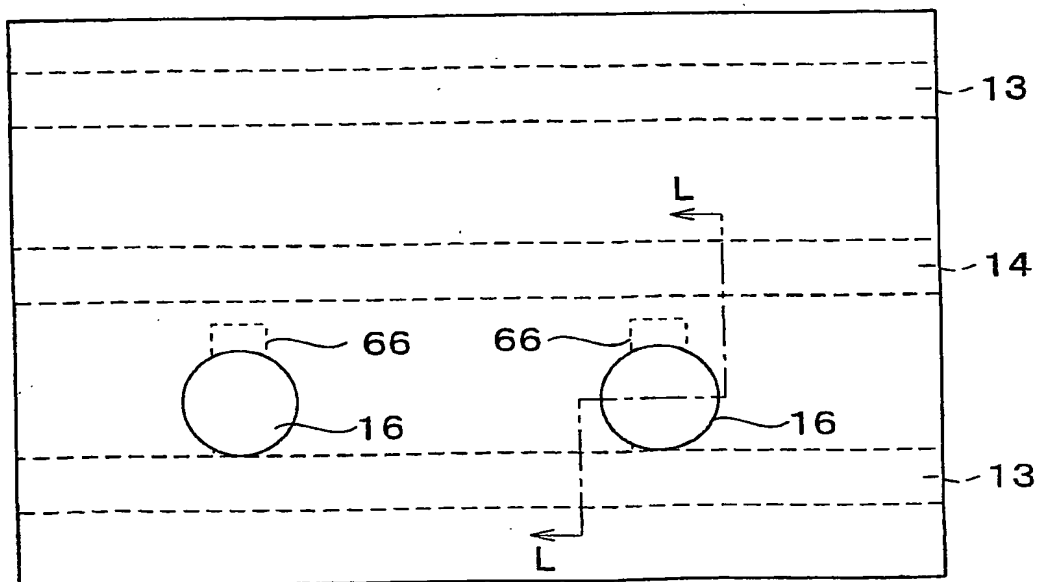


FIG. 23

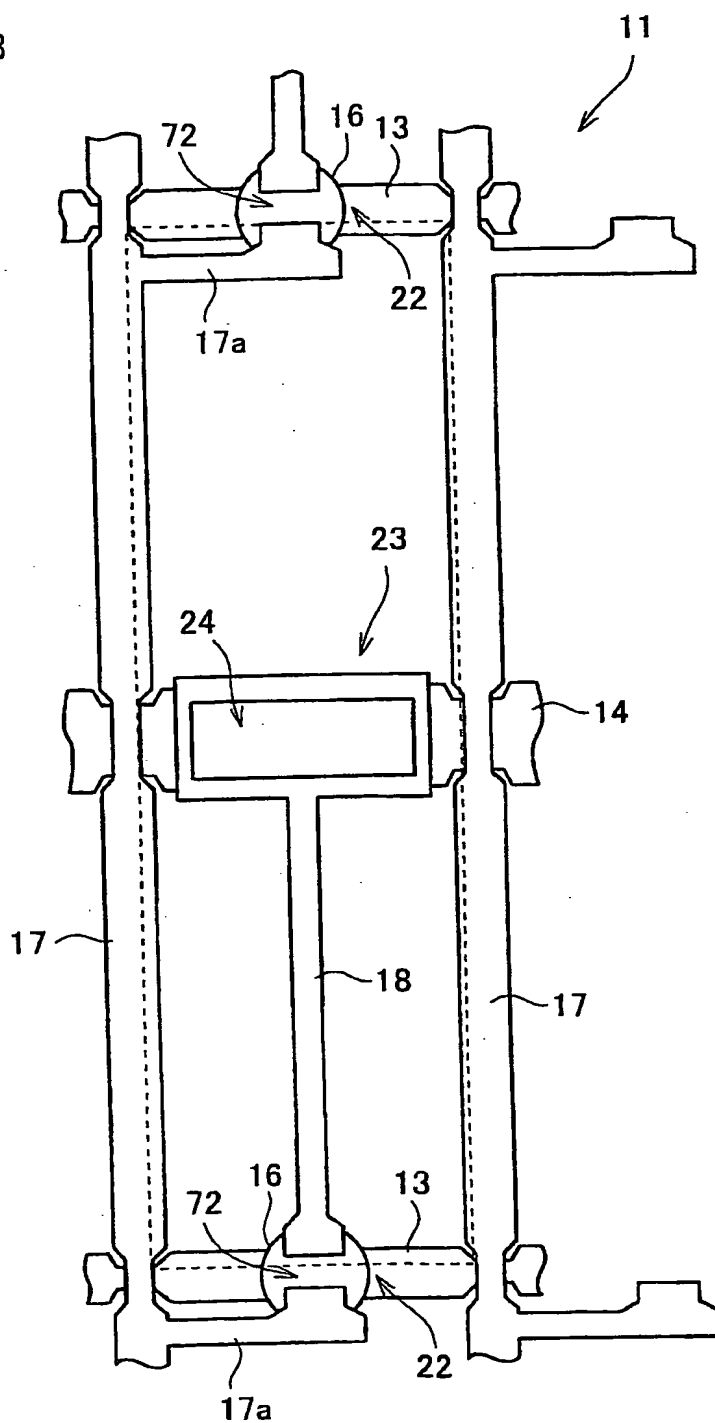


FIG. 24

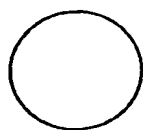


FIG. 25(a)

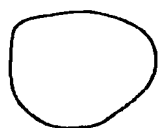


FIG. 25(b)



FIG. 25(c)



FIG. 26(a)

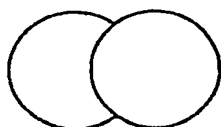


FIG. 26(b)

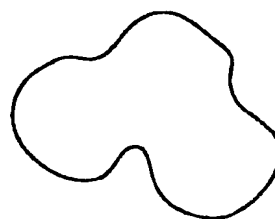
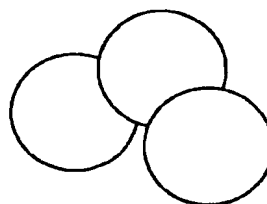


FIG. 27(a)

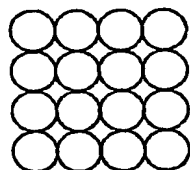


FIG. 27(b)

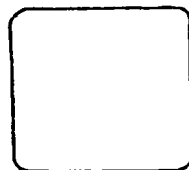


FIG. 28

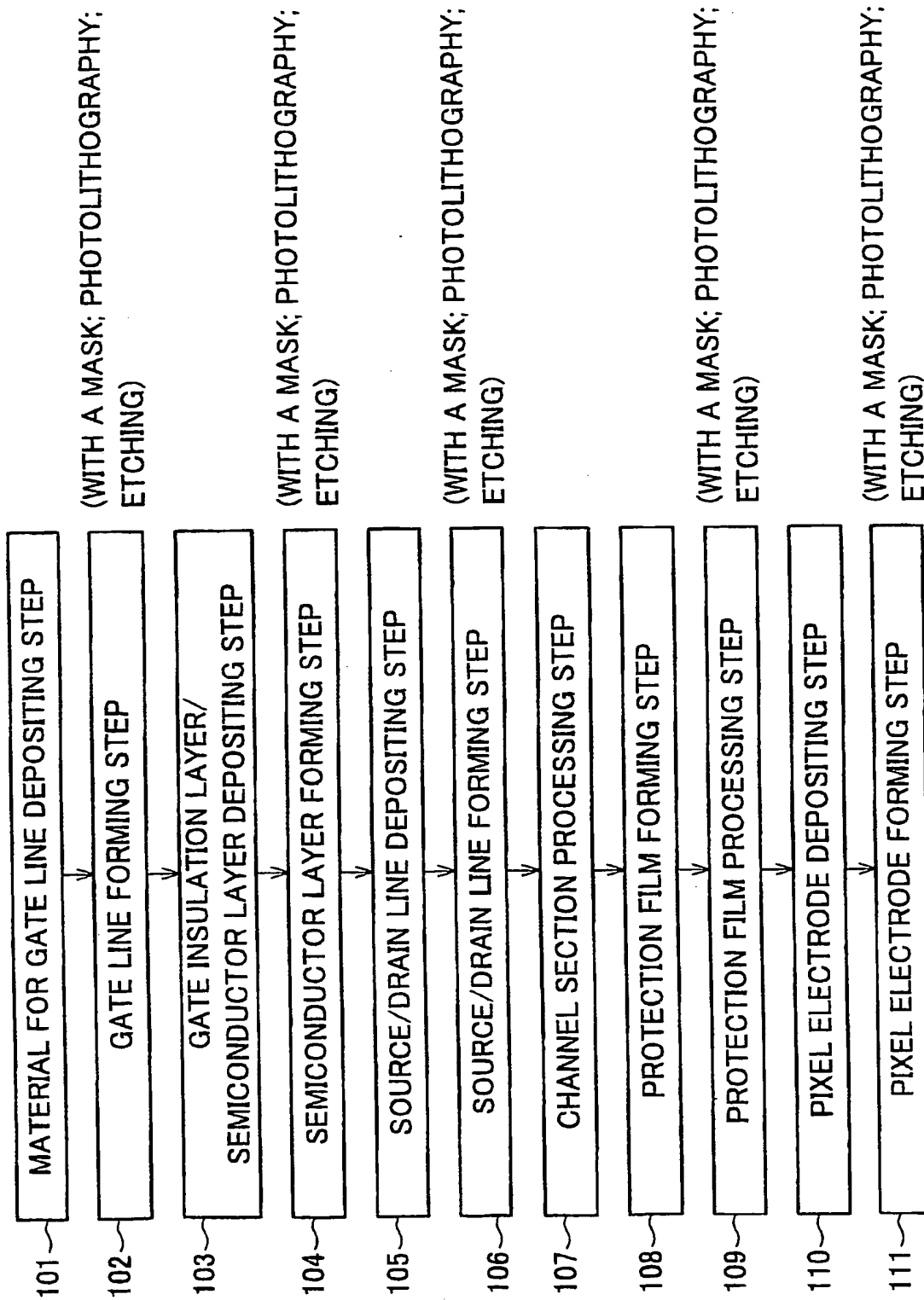


FIG. 29

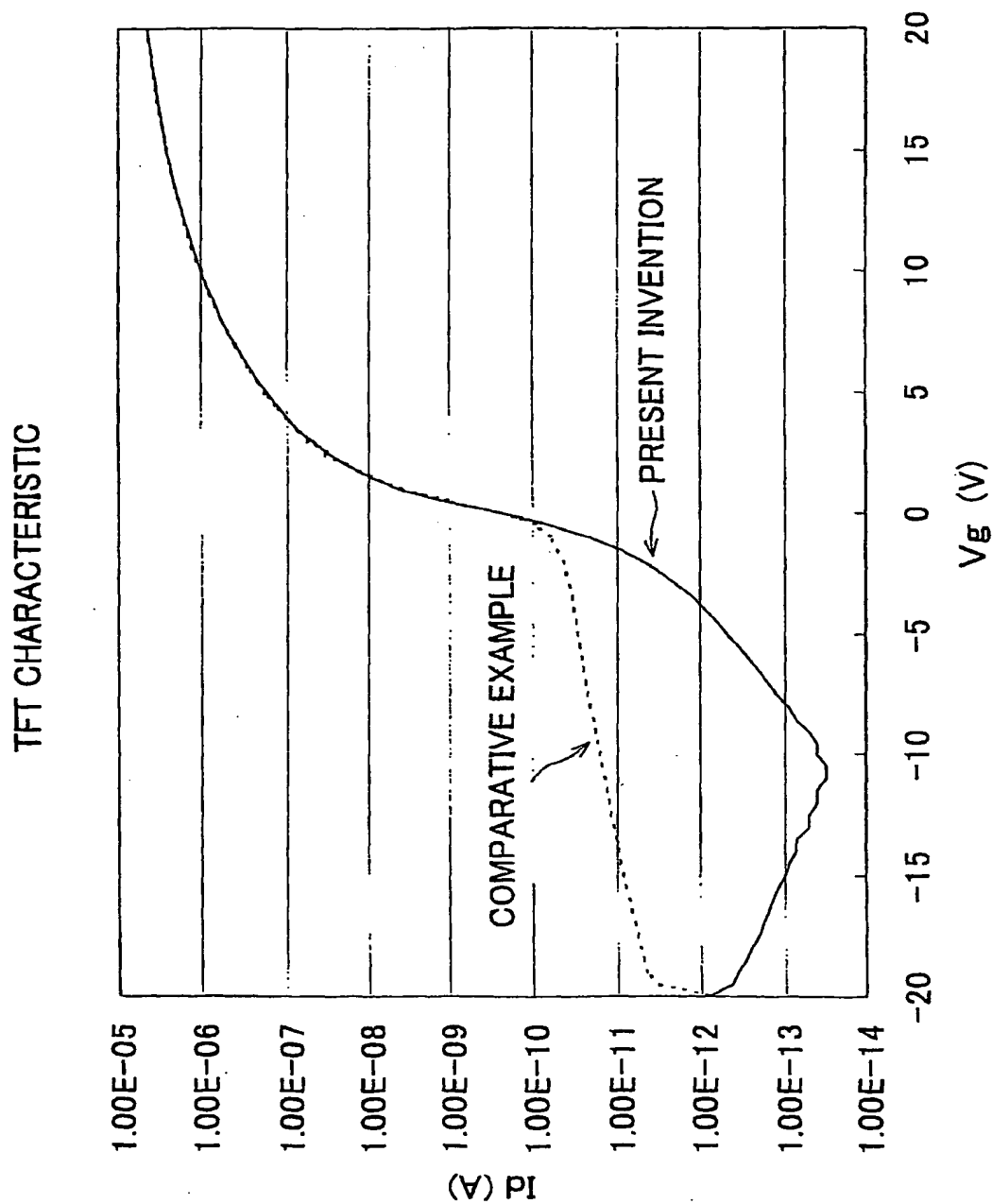


FIG. 30

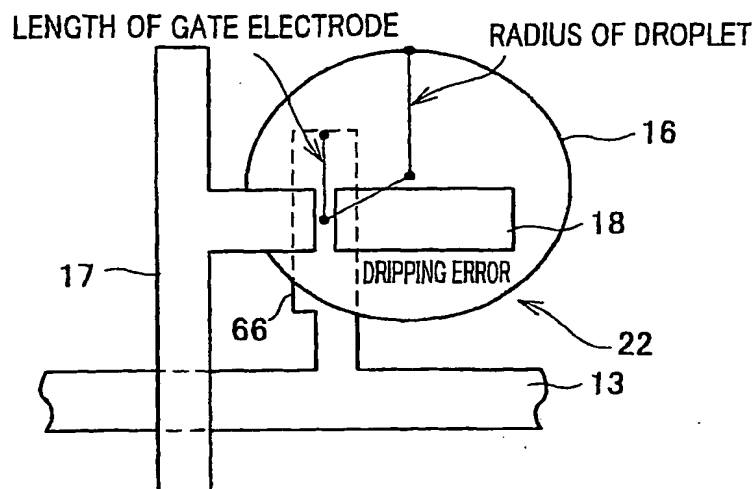


FIG. 31

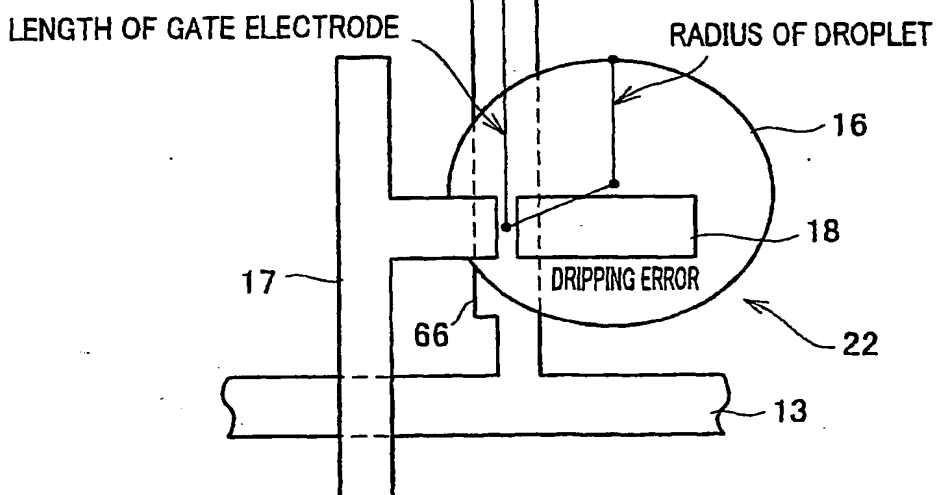


FIG. 32

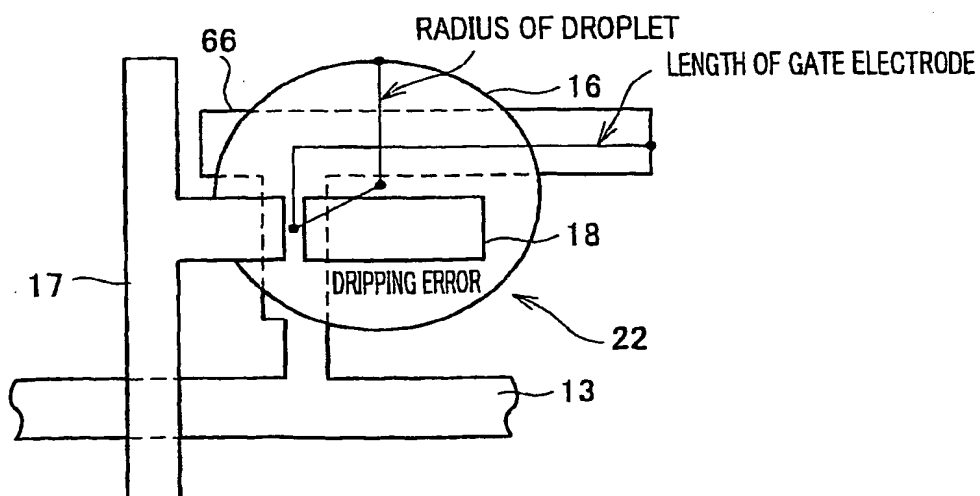


FIG. 33

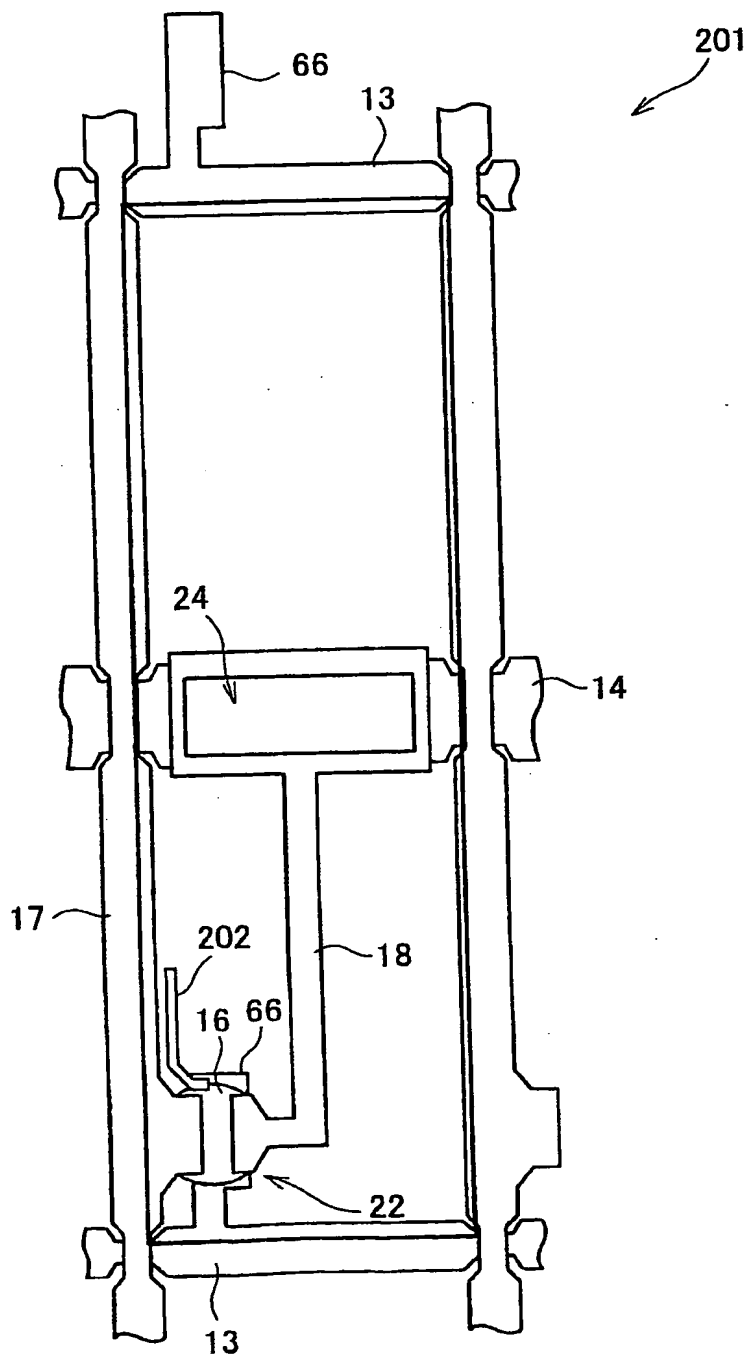


FIG. 34

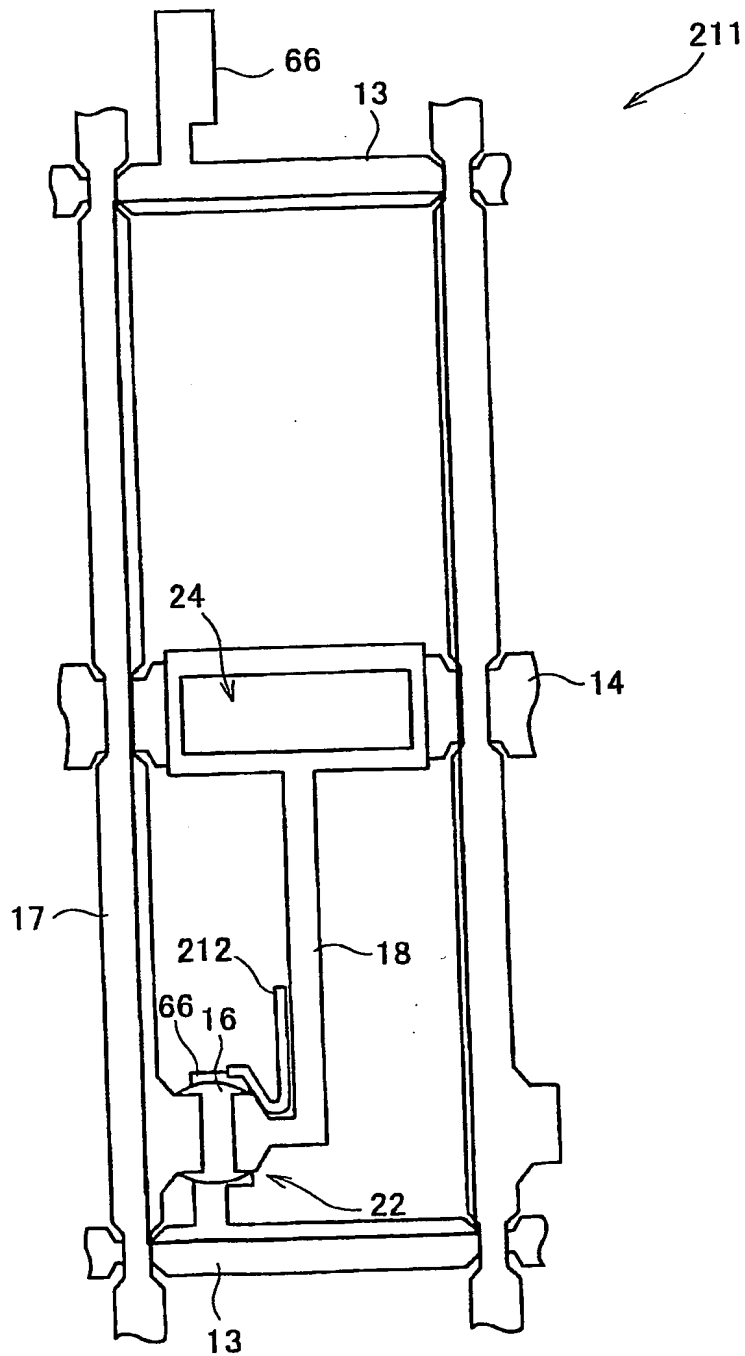


FIG. 35

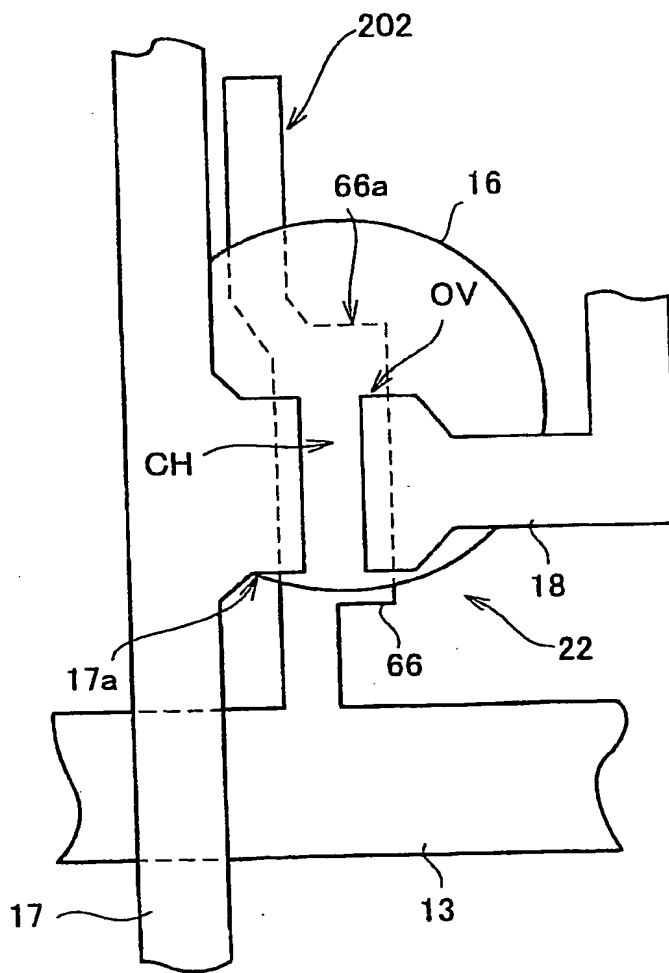


FIG. 36

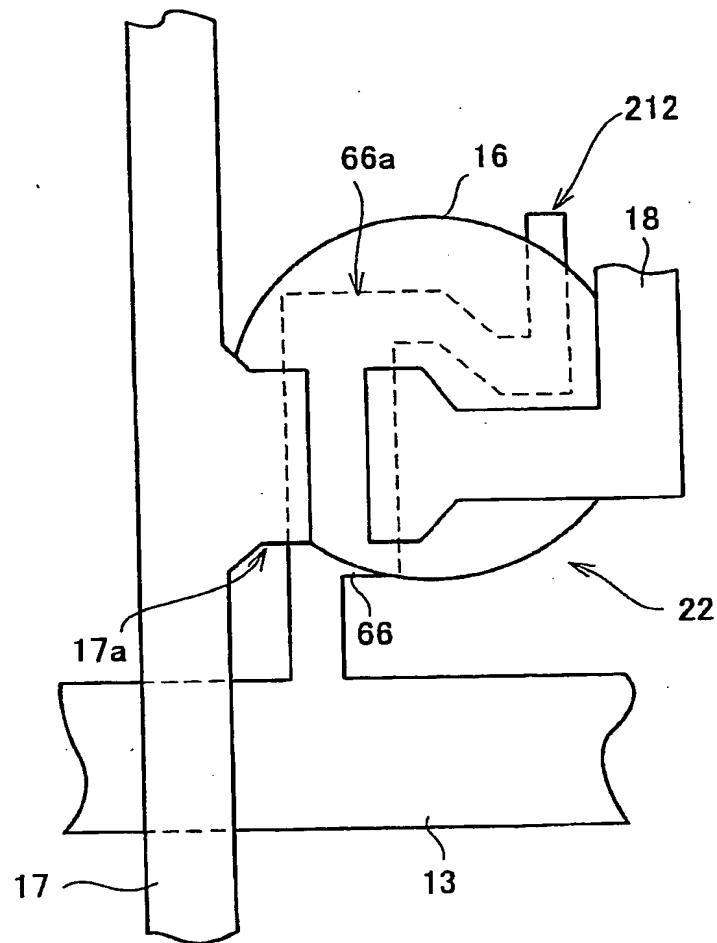
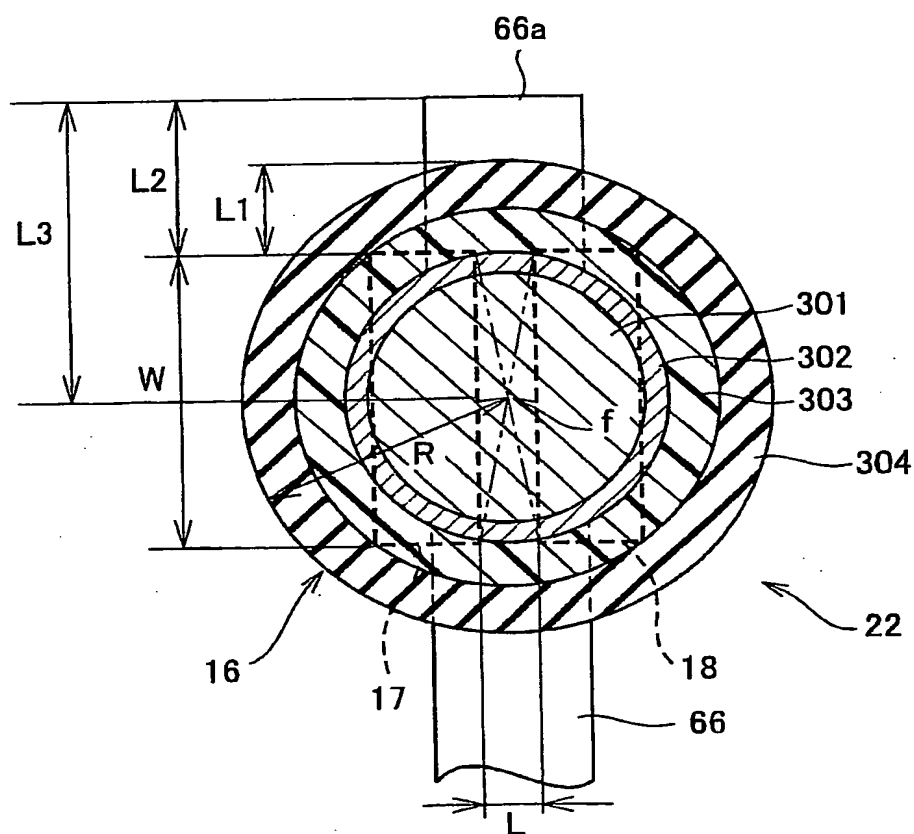
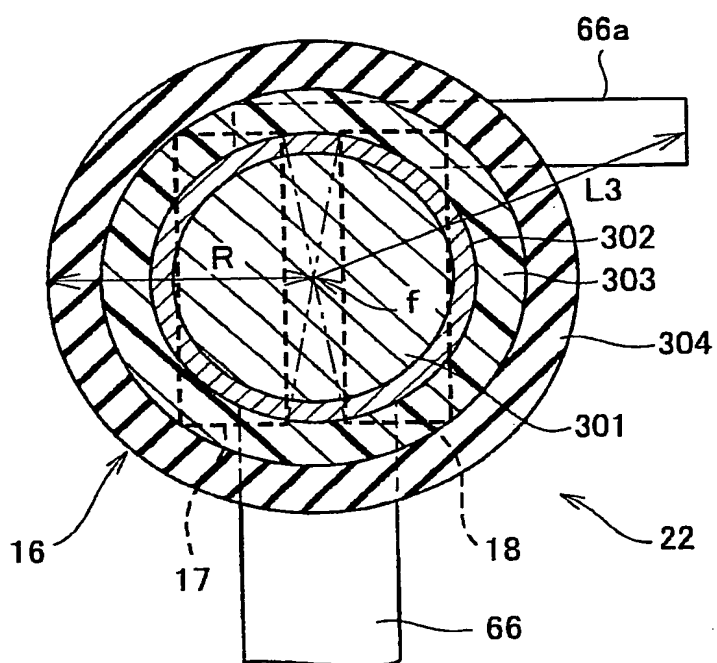


FIG. 37



$$\begin{aligned} L_1 &> \Delta_1 + \Delta_2 \\ L_2 &> \Delta_1 + 2\Delta_2 \\ L_3 &> r + \Delta_1 + 2\Delta_2 \end{aligned}$$

FIG. 38



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FIG. 39(a)

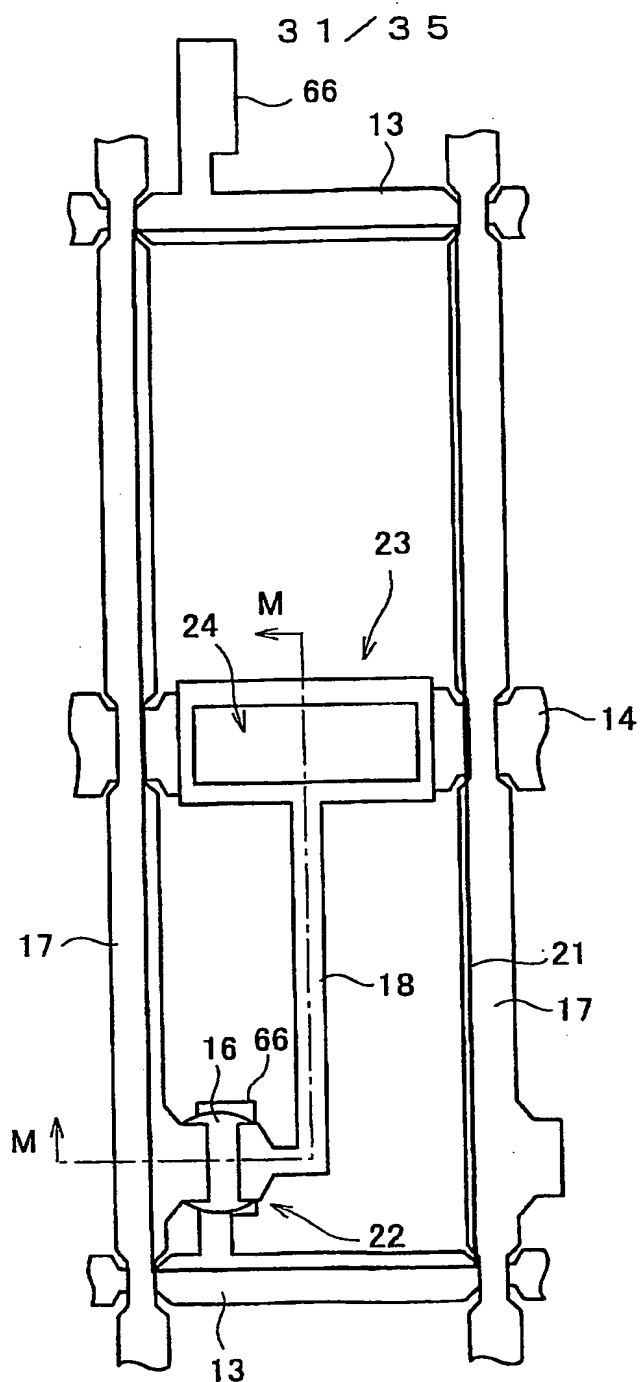


FIG. 39(b)

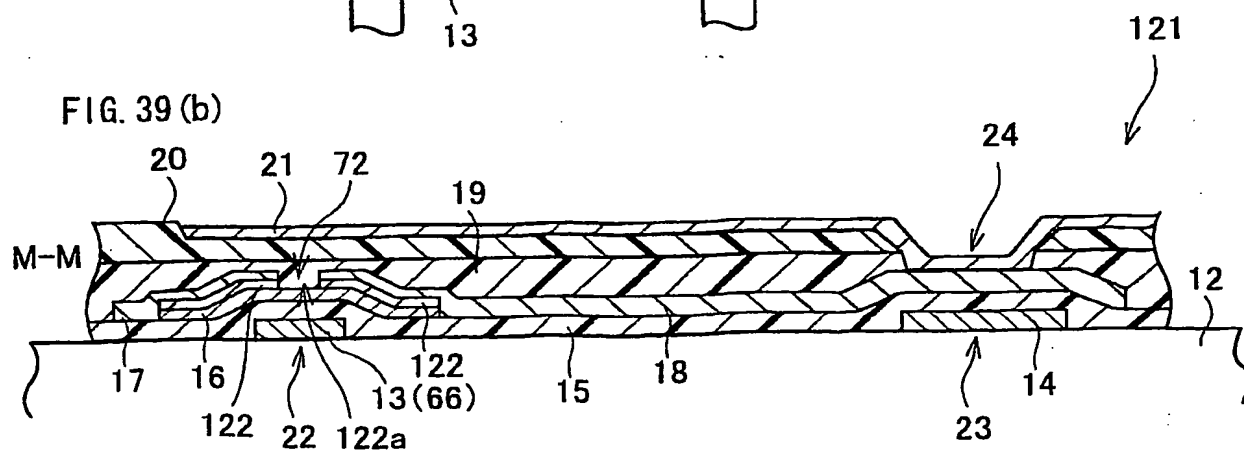


FIG. 40

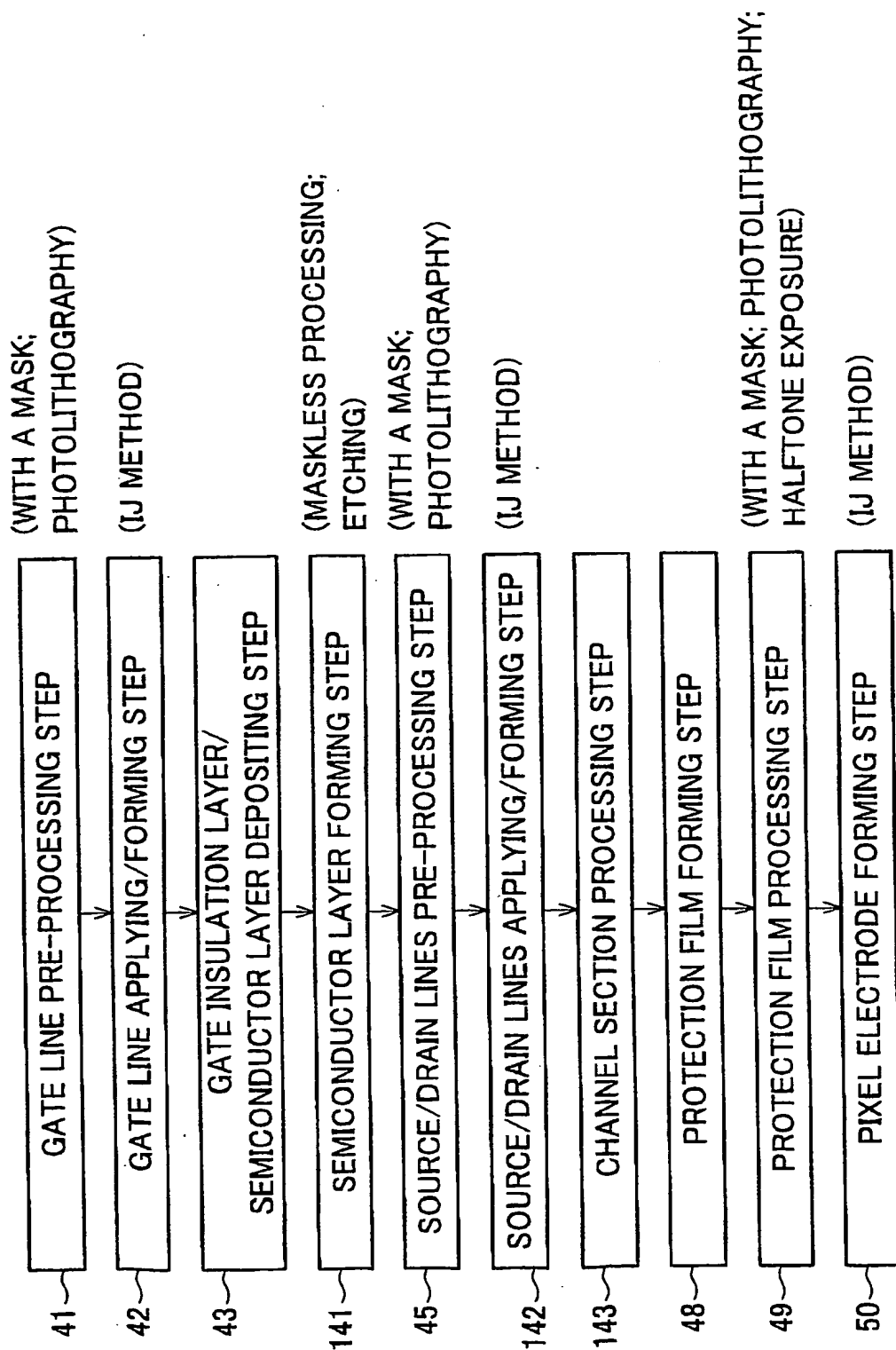


FIG. 41 (a) (SEMICONDUCTOR FORMING STEP)

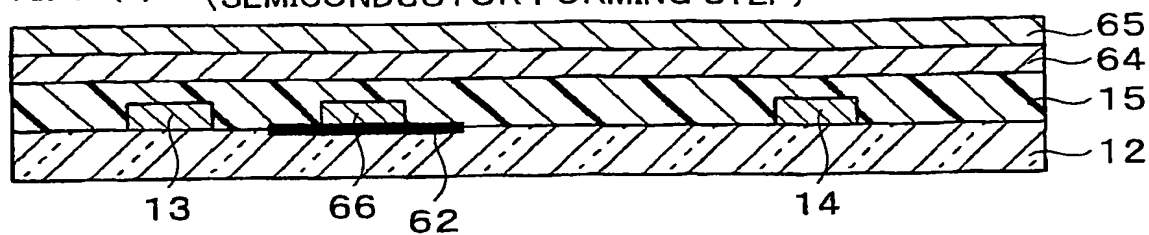


FIG. 41 (b)

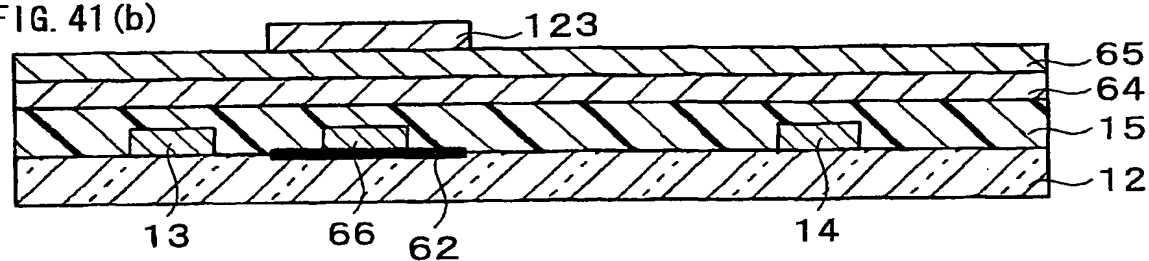
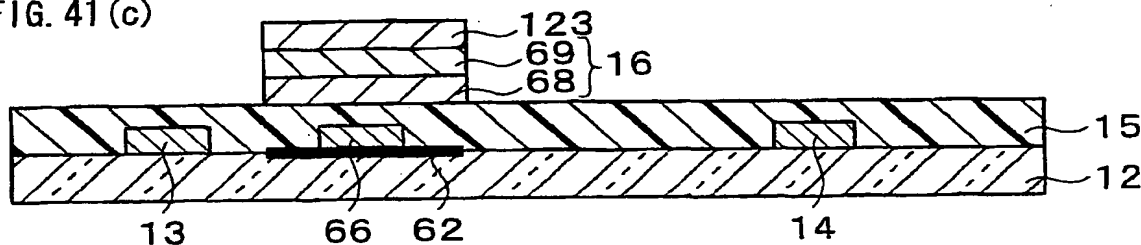


FIG. 41 (c)



(N-N CROSS-SECTION)

FIG. 41 (d)

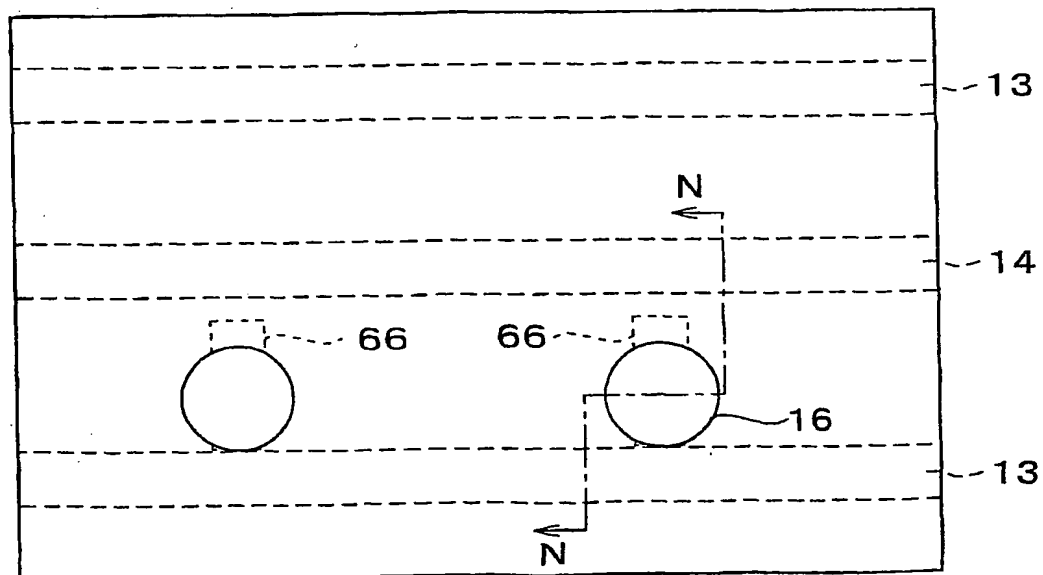


FIG. 42 (a) (SOURCE/DRAIN LINE PRE-PROCESSING STEP)

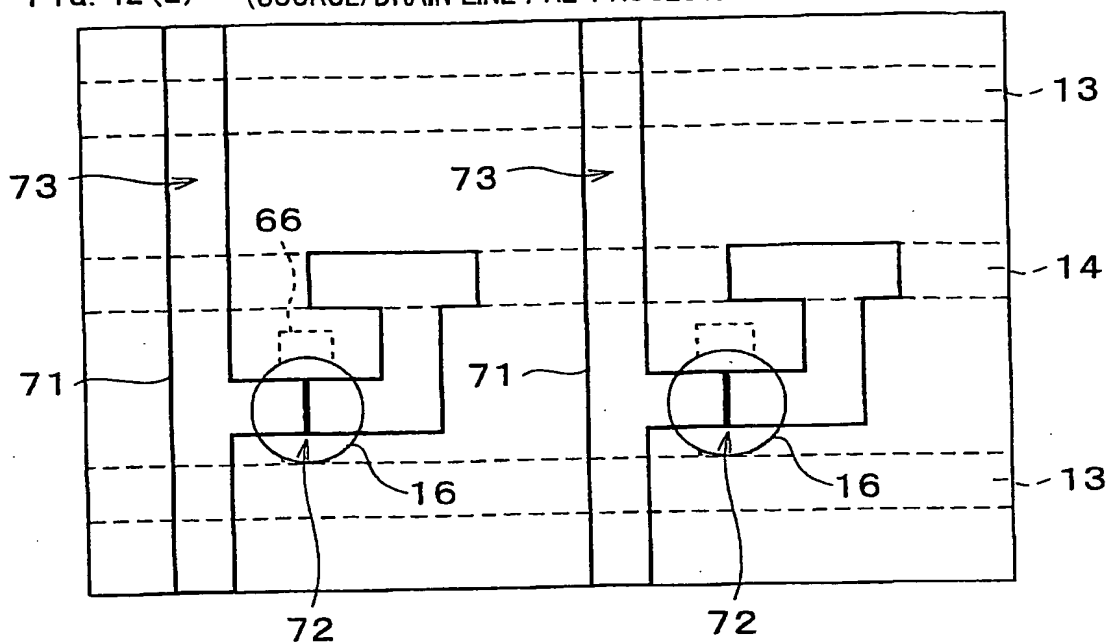


FIG. 42(b) (SOURCE/DRAIN LINE FORMING STEP)

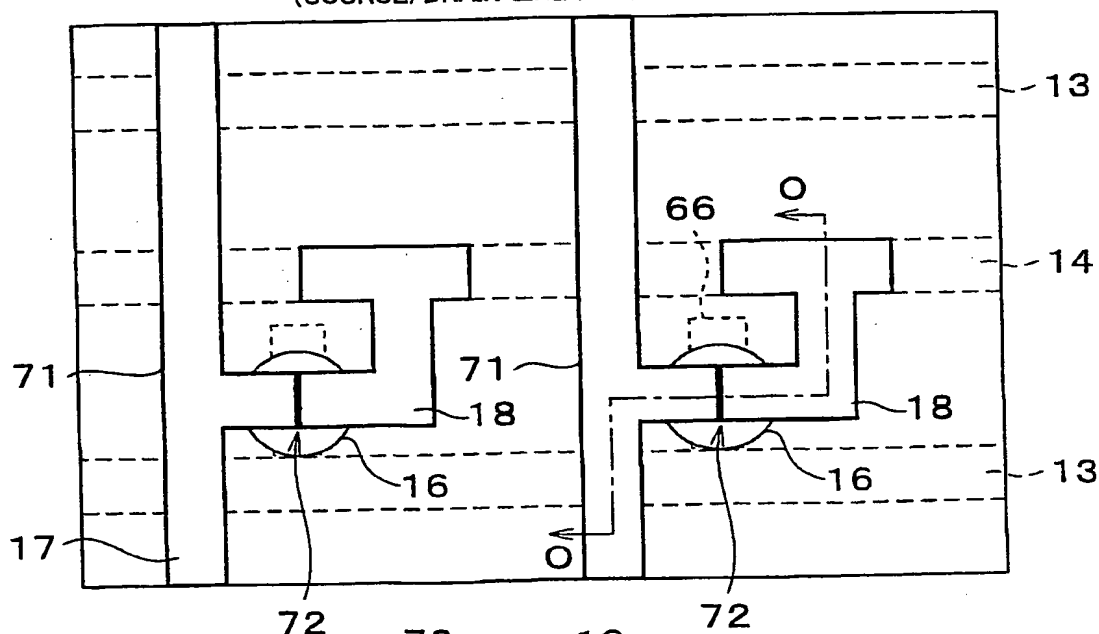


FIG. 42(c)

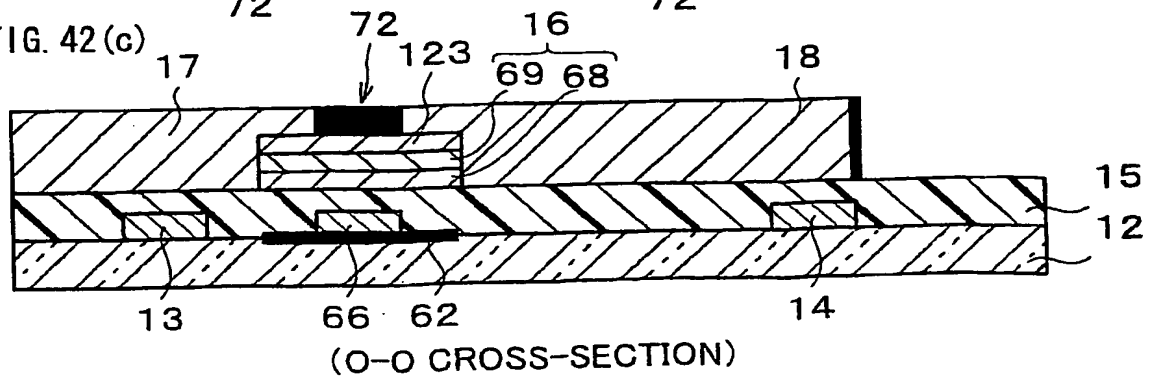


FIG. 43(a)

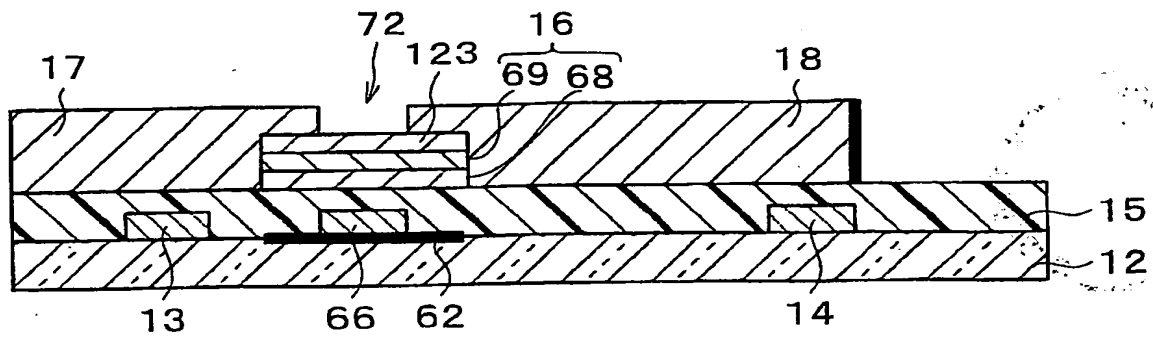


FIG. 43(b)

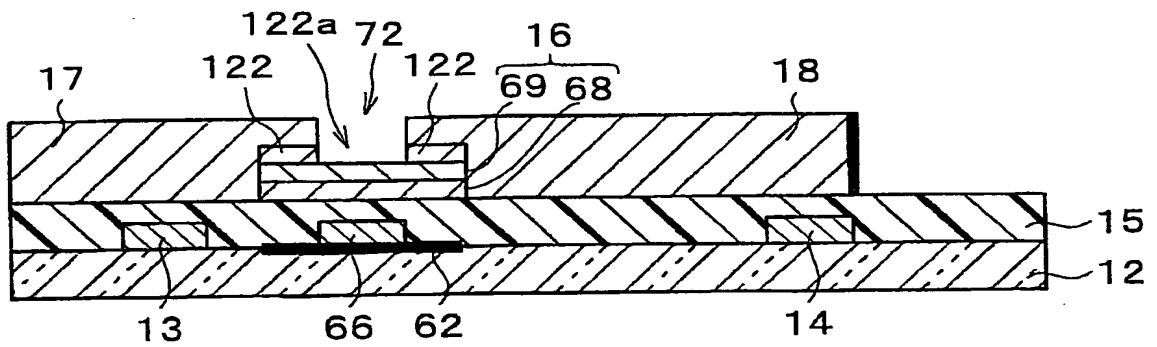


FIG. 43(c)

